

Errata Sheet

1. Introduction

This note describes an issue seen with the data and data Ready (D-CK) Timing.

This document applies to the:

- TS86101 10-bit MUXDAC
 - TS86101G2BCG
 - TS86101G2BVGL
 - TS86101G2BMGS
 - TS86101G2BMGS9NB1

For further assistance please contact hotline-bdc@e2v.com

2. Description of Problem

The timing values Tsetup and Thold marked in the datasheet TS86101 (0992-BDC-04/09) have been found to be incorrect.

Hence the [Figure 5-2](#) and [Figure 5-3](#) in the datasheet are also incorrect.

The correct value for Tsetup has been found to be 1.2 ns min and Thold has been found to be 0.5 ns min.

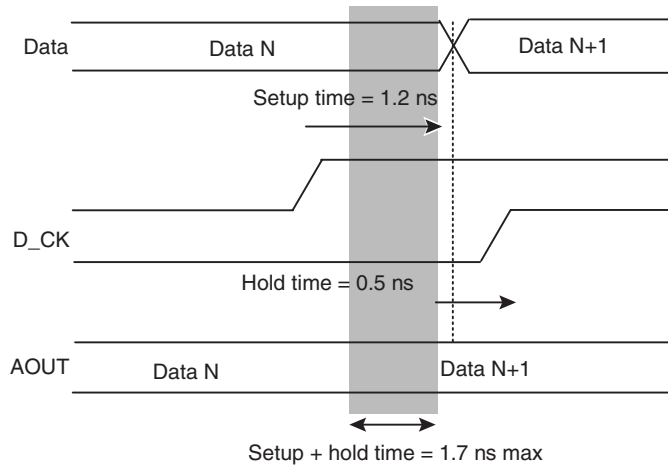
These values are found in Table 2-4 of the datasheet.

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for the latest version of the datasheet

TS86101 / 10 bit MUXDAC

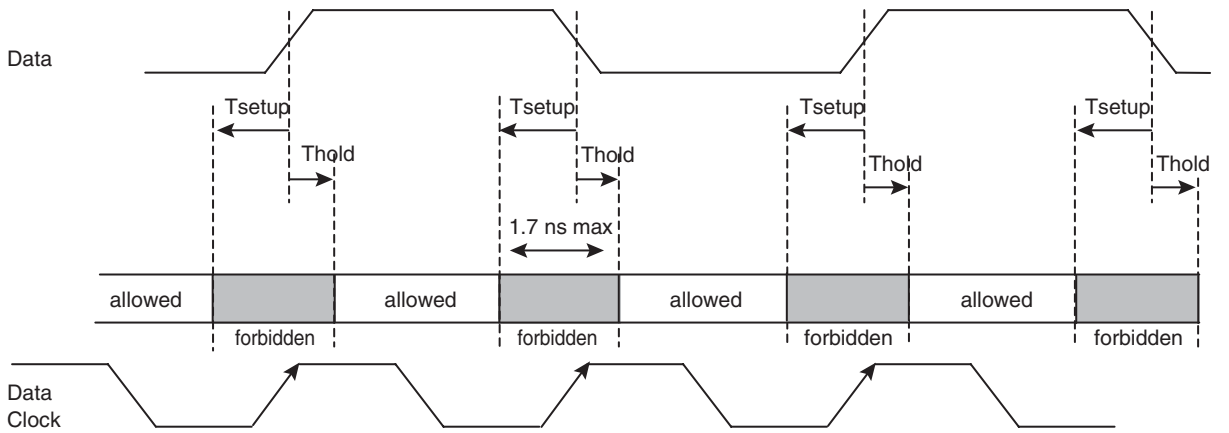
Correct [Figure 5-2](#) Data to Data Ready (D-CK) Timing.

Figure 5-2. Data to Data Ready (D-CK) Timing



Correct [Figure 5-3](#) Data to Data Clock Forbidden Area

Figure 5-3. Data to Data Clock Forbidden Area



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