Qualification report 12bit 4.5Gsps MuxDAC
EV12DS400A – VN62A – FpBGA 196 - THIMS

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1. INTRODUCTION

This document presents the results of all tests that have been carried out by e2v Grenoble to qualify the EV12DS400A family - 12bit 4.5Gsps MuxDAC - in FpBGA 196 package according to the following document:

NE 31S 212 082: Qualification plan - 12bit 4.5Gsps MuxDAC - VN62A - EV12DS400A - FpBGA 196 – THIMS

2. APPLICABLE DOCUMENTS

- NE.31S.212082 Qualification plan - 12bit 4.5Gsps MuxDAC - VN62A - EV12DS400A - FpBGA 196 – THIMS
- SQ.32S.07680 GUIDE DE QUALIFICATION DES PRODUITS HRS
- JEDEC Standard Global standards for the microelectronics industry

3. PRODUCTS DESCRIPTION

3.1 DIE INFORMATION

Product	EV12DS400A
Mask	VN62A
Process name	B7HF200
Process type	200Ghz SiGe Bipolar
Die size	4.58 mm x 4.58 mm (21 mm²)
Passivation	SiO2 (0.3 µm) & SiN (0.55 µm)
Die thickness	300 µm
Last metallization layer	Au (500nm) / Pt (60nm) / Ti (60nm)

3.2 PACKAGE INFORMATION

Package	FpBGA 196
Package outline	15 x 15 x 1.2 mm
Pitch	1.00 mm
Die attach material	Ablebond 2000B (green)
Substrate	SCC PHP900 & MCT
Wire	Au 25 µm
Mold Compound	EME G760V (green)
Solder Ball	Sn62/Pb36/Ag2 or SAC305 (Pb-Free)
Flux	WSD 3810 - Umicore
Moisture Level	3 (peak 235°C & 260°C)
P (dissipated power in Watt)	2.6 Watt (in 4:1 MUX)

3.3 LOCATION INFORMATION

Wafer fab	Infineon (Germany)
Assy plant	Unisem Batam (Indonesia)
Testing plant	e2v (Grenoble)

4. SYNTHESIS RESULTS

TEST *Acceptable criteria*	METHOD *Condition*	Sample	Fail	Status
Construction analysis *Infineon B7HF 200 specifications*	MIL-STD-883 TM2018 *Mask VN62A*	6	0	***Pass***
ESD HBM *ATE program*	JESD22-A114E *Class 1C (1000V to < 2000V*	3	0	***Pass***
Operating Life Test *ATE program*	MIL-STD-883 TM1005 *1000 Hrs / Tj 167°C*	48	0	***Pass***
ESD MM *ATE program*	JESD22-A115-C *Class M2 (100V to < 200V*	3	0	***Pass***
LATCH UP *ATE program*	JEDEC 78B *Class I* *Class II*	3 3	0 0	***Pass***
Moisture sensitivity Level 3 *ATE program* *Ultrasound scan & transmission*	JSTD-020D *Level 3 /30°C 60%RH 192H peak 260°C*	24	0	***Pass***
Temp. Humidity with Bias* *ATE program*	JESD22-A101 *1000Hrs / 85°C/85% RH/ 7.12Psi*	24*	0	***Pass***
Temperature Cycle* *ATE program* *Visual inspection*	JESD22-A104 *500 cy A/A -65°C / 150°*	24*	0	***Pass***
Accelerated Moisture resistance – Unbiased Autoclave *ATE program*	JESD22-A102-C *121°C/2atm/100%RH / 168Hrs*	Done by similarity**		***Pass***
Highly Accelerated Stress Test *ATE program* *Visual inspection*	JESD22-A110 *96H 130°C/85%RH/2atm Unbiased*	Done by similarity**		***Pass***
High Temperature Storage *ATE program*	JESD22-A103-C *1000Hrs / 150°C*	Done by similarity**		***Pass***
Outline measurements *Package spec*	FpBGA package outline *Package spec*	Done by similarity**		***Pass***
Ball Shear *Visual inspection*	JESD22-B117 & AEC-Q100-010 *Min acceptable=500g*	Done by similarity**		***Pass***
Package Construction analysis *Internal visual*	Microsections *Package spec*	Done by similarity**		***Pass***

*Devices Issued from MSL3
**Qualification based on results from same package and die family

5. GENERAL CONCLUSION

The following products have passed with success all tests as defined in test plan ref: NE 31S 212 082.

Products	Package	Termination finish	Max. peak reflow	Temperature range
EV12DS400ACZP	FpBGA 196	Sn62/Pb36/Ag2	235°C	"C" Grade 0°C < Tc ; Tj < 90°C
EV12DS400ACZPY		Sn96.5/Ag3/Cu0.5	260°C	
EV12DS400AVZP		Sn62/Pb36/Ag2	235°C	"V" Grade -40°C < Tc ; Tj < 110°C
EV12DS400AVZPY		Sn96.5/Ag3/Cu0.5	260°C	
EV12DS400AMZP		Sn62/Pb36/Ag2	235°C	"M" Grade -55°C < Tc, Tj < 125°C
EV12DS400AMZPY		Sn96.5/Ag3/Cu0.5	260°C	

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6. ASSEMBLY LOT INFORMATION

Mask	Diffusion lot	Assy lot ID / WO	Date Code
VN62A	**RU516515**	**4719043 / 4 / 5**	**1526**

7. TEST RESULTS

7.1 VN62A die results

7.1.1 Construction analysis

TEST *Acceptable criteria*	**METHOD** *Condition*	**Sample**	**Fail**	**Status**
Construction analysis *Infineon B7HF 200 specifications*	MIL-STD-883 TM2018 *Mask VN62A*	6	0	***Pass***

Done by SERMA Technologies, see report "AF15-3287-Report .pdf".

7.1.2 Operating Life Test

TEST *Acceptable criteria*	**METHOD** *Condition*	**Sample**	**Fail**	**Status**
Operating Life Test *ATE program*	MIL-STD-883 TM1005 *1000 Hrs / Tj 167°C*	48	0	***Pass***

Parts issued from a lot of 12 wafers VN62A RU516515-VN62A_S1423A11

7.1.3 ESD HBM

TEST *Acceptable criteria*	**METHOD** *Condition*	**Sample**	**Fail**	**Status**
ESD HBM *ATE program*	JESD22-A114E *Class 1C (1000V to < 2000V*	3	0	***Pass***

ESD HBM Qty		**ESD Stress**	**STS**	**e2v final Amb. Elct.**
9		**9**	**0**	**3**
2		**250V**	**stressed**	**ok**
3		**250V**	**stressed**	**ok**
4		**250V**	**stressed**	**ok**
5		**500V**	**stressed**	**ok**
6		**500V**	**stressed**	**ok**
7		**500V**	**stressed**	**ok**
8		**1000V**	**stressed**	**ok**
9		**1000V**	**stressed**	**ok**
10		**1000V**	**stressed**	**ok**

Done by STS USA on a lot with **DC 1345**, see report "171450 HBM Report Rev B- E2V - EV12DS400A_THIMS.PDF".

7.1.4 ESD MM

TEST *Acceptable criteria*	METHOD *Condition*	Sample	Fail	Status
ESD MM *ATE program*	JESD22-A115-C *Class M2 (100V to < 200V*	3	0	***Pass***

ESD MM Qty		ESD Stress	STS	e2v final Amb. Elct.
9		9	0	3
11		100V	stressed	ok
12		100V	stressed	ok
13		100V	stressed	ok
14		200V	stressed	Fail O/S
15		200V	stressed	Fail O/S
16		200V	stressed	Fail O/S
17		400V	stressed	Fail O/S
18		400V	stressed	Fail O/S
19		400V	stressed	Fail O/S

Done by STS USA on a lot with **DC 1345**, see report "171451 MM Report Rev B- E2V - EV12DS400A_THIMS.PDF".

7.1.5 LATCH UP

TEST *Acceptable criteria*	METHOD *Condition*	Sample	Fail	Status
LATCH UP *ATE program*	JEDEC 78B *Class I* *Class II*	 3 3	 0 0	***Pass***

LU Qty		LU Stress	STS	e2v final Amb. Elct.
6		3+3	0	3+3
20		Ambient Temp.	stressed	ok
21		Ambient Temp.	stressed	ok
22		Ambient Temp.	stressed	ok
23		High Temp.	stressed	ok
24		High Temp.	stressed	ok
25		High Temp.	stressed	ok

Done by STS USA on a lot with **DC 1345**, see report "171459 Latch Up Test Report Rev B - E2V-EV12DS400A-THIMS.PDF".

Conclusion:
EV12DS400Axxx product mask VN62A has successfully passed SEM analysis, Life test, ESD and Latch up tests.

7.2 FpBGA 196 Package tests

In order to test the package FpBGA 196, the following tests have been done sequentially on the same 24 parts issued from the original lot with **DC 1526**:

Thermal test – *Phase 1*					
Step	**Test**	**Method**	**Condition**	**CA / CR**	**Fail / Ok**
1	Electrical test	Prog: EV12DS400A	Ambient temperature	24 / 0	***Pass***
2	**Moisture sensitivity Level 3**	JSTD-020D	Level 3 /30°C 60%RH 192H peak 260°C	24 / 0	***Pass***
3	Electrical test	Prog: EV12DS400A	Ambient temperature	24 / 0	***Pass***
4	**Temp. Humidity with Bias**	JESD22-A101	1000Hrs / 85°C/85% RH/ 7.12Psi	24 / 0	***Pass***
5	Electrical test	Prog: EV12DS400A	Ambient temperature	24 / 0	***Pass***
Then for reliability evaluation (on same devices) - *Phase 2*					
6	**Temperature Cycle**	JESD22-A104 / MIL -STD-883 TM1010	500 cy A/A -65°C / 150°	24 / 0	***Pass***
7	Electrical test	Prog: EV12DS400A	Ambient temperature	24 / 0	***Pass***
8	Ext.Visual insp.	ESCC 20500		24 / 0	***Pass***

Tests 2 **MSL 3** and 4 **THB** were done by HIREX, France, see report “PVT_07308_01 (MSL).pdf” for test 2 and “Feuille Suivi THB 1000Hrs.pdf” for test 4.

Conclusion:

EV12DS400Axxx products with package FpBGA have successfully passed temperature and reliability tests.