

Datasheet - *Preliminary Specification*

Features

- Dual-e600 Power Architecture™ Processor Cores
- PD Typically 23.9W at 1.25 GHz ($V_{DD} = 1.05V$) ; 32.1W at 1.5 GHz ($V_{DD} = 1.1V$)
- Selectable MPX Bus up to 600MHz (64 bits)
- Integrated L1: 32 KB Instruction and 32 KB Data Cache (Per Core with Parity Protection)
- Integrated L2: 1 MB Per Core with Optional ECC
- Serial RapidIO Interface 1x, 4x (1.25, 2.5 and 3.125Gbaud)
- PCI Express Interface 1x, 4x or 8x (2.5Gbaud/lane)
- Ethernet Interface : Four 10/100/1000 Ethernet Controllers
- Memory Controller : Support Dual 64-bit DDR and DDRII with up to 600 MHz Data Rate with ECC
- Up to 16GB Per Memory Controller.
- DMA Controller : Four Independent Channels with Bandwith Control per Channel
- f_{INT} Max = 1500 MHz
- f_{BUS} Max = 600 MHz



Overview

The PC8641 processor family integrates either one or two Power Architecture e600 processor cores with system logic required for networking, storage, wireless infrastructure, and general-purpose embedded applications. The PC8641 integrates one e600 core while the PC8641D integrates two cores.

This section provides a high-level overview of the PC8641 and PC8641D features. When referring to the PC8641 throughout the document, the functionality described applies to both the PC8641 and the PC8641D. Any differences specific to the PC8641D are noted.

[Figure 1-1 on page 2](#) shows the major functional units within the PC8641 and PC8641D. The major difference between the PC8641 and PC8641D is that there are two cores on the PC8641D.

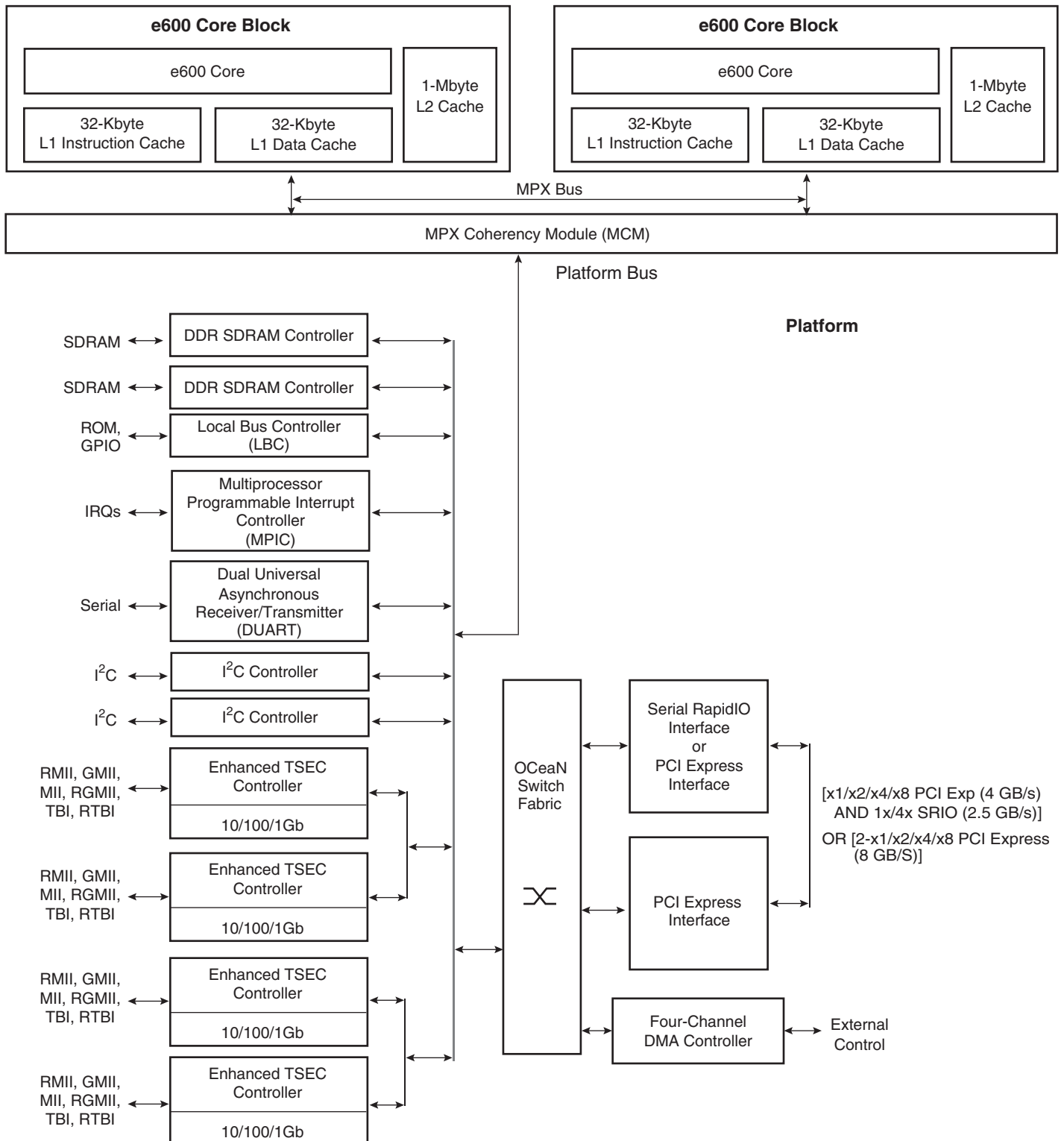
Screening

- Full Military Temperature Range ($T_C = -55^\circ C$, $T_J = +125^\circ C$)
- Industrial Temperature Range ($T_C = -40^\circ C$, $T_J = +110^\circ C$)

PC8641 and PC8641D [Preliminary]

1. Block Diagram

Figure 1-1. PC8641 and PC8641D



2. Key Features

The following lists an overview of the PC8641 key feature set:

- Major features of the e600 core are as follows:
 - High-performance, 32-bit superscalar microprocessor that implements the Power Architecture
 - Eleven independent execution units and three register files
 - Branch processing unit (BPU)
 - Four integer units (IUs) that share 32 GPRs for integer operands
 - 64-bit floating-point unit (FPU)
 - Four vector units and a 32-entry vector register file (VRs)
 - Three-stage load/store unit (LSU)
 - Three issue queues, FIQ, VIQ, and GIQ, can accept as many as one, two, and three instructions, respectively, in a cycle.
 - Rename buffers
 - Dispatch unit
 - Completion unit
 - Two separate 32-Kbyte instruction and data level 1 (L1) caches
 - Integrated 1-Mbyte, eight-way set-associative unified instruction and data level 2 (L2) cache with ECC
 - 36-bit real addressing
 - Separate memory management units (MMUs) for instructions and data
 - Multiprocessing support features
 - Power and thermal management
 - Performance monitor
 - In-system testability and debugging features
 - Reliability and serviceability
- MPX coherency module (MCM)
 - Ten local address windows plus two default windows
 - Optional low memory offset mode for core 1 to allow for address disambiguation
- Address translation and mapping units (ATMUs)
 - Eight local access windows define mapping within local 36-bit address space
 - Inbound and outbound ATMUs map to larger external address spaces
 - Three inbound windows plus a configuration window on PCI Express
 - Four inbound windows plus a default window on serial RapidIO
 - Four outbound windows plus default translation for PCI Express
 - Eight outbound windows plus default translation for serial RapidIO with segmentation and sub-segmentation support
- DDR memory controllers
 - Dual 64-bit memory controllers (72-bit with ECC)
 - Support of up to a 333-MHz clock rate and a 667-MHz DDR2 SDRAM
 - Support for DDR, DDR2 SDRAM

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- Up to 16 Gbytes per memory controller
- Cache line and page interleaving between memory controllers.
- Serial RapidIO interface unit
 - Supports RapidIO Interconnect Specification, Revision 1.2
 - Both 1x and 4x LP-Serial link interfaces
 - Transmission rates of 1.25-, 2.5-, and 3.125-Gbaud (data rates of 1.0-, 2.0-, and 2.5-Gbps) per lane
 - RapidIO-compliant message unit
 - RapidIO atomic transactions to the memory controller
- PCI Express interface
 - PCI Express 1.0a compatible
 - Supports x1, x2, x4, and x8 link widths
 - 2.5 Gbaud, 2.0 Gbps lane
- Four enhanced three-speed Ethernet controllers (eTSECs)
 - Three-speed support (10/100/1000 Mbps)
 - Four IEEE® 802.3, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab compliant controllers
 - Support of the following physical interfaces: MII, RMII, GMII, RGMII, TBI, and RTBI
 - Support a full-duplex FIFO mode for high-efficiency ASIC connectivity
 - TCP/IP off-load
 - Header parsing
 - Quality of service support
 - VLAN insertion and deletion
 - MAC address recognition
 - Buffer descriptors are backward compatible with PowerQUICC II and PowerQUICC III programming models
 - RMON statistics support
 - MII management interface for control and status
- Programmable interrupt controller (PIC)
 - Programming model is compliant with the OpenPIC architecture
 - Supports 16 programmable interrupt and processor task priority levels
 - Supports 12 discrete external interrupts and 48 internal interrupts
 - Eight global high resolution timers/counters that can generate interrupts
 - Allows processors to interrupt each other with 32b messages
 - Support for PCI-Express message-shared interrupts (MSIs)
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data operating at up to 166 MHz
 - Eight chip selects support eight external slaves
- Integrated DMA controller
 - Four-channel controller
 - All channels accessible by both the local and the remote masters

- Supports transfers to or from any local memory or I/O port
- Ability to start and flow control each DMA channel from external 3-pin interface
- Device performance monitor
 - Supports eight 32-bit counters that count the occurrence of selected events
 - Ability to count up to 512 counter-specific events
 - Supports 64 reference events that can be counted on any of the 8 counters
 - Supports duration and quantity threshold counting
 - Burstiness feature that permits counting of burst events with a programmable time between bursts
 - Triggering and chaining capability
 - Ability to generate an interrupt on overflow
- Dual I²C controllers
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset via the I²C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I²C addressing mode
 - Data integrity checked with preamble signature and CRC
- DUART
 - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
 - Programming model compatible with the original 16450 UART and the PC16550D
- IEEE 1149.1-compliant, JTAG boundary scan
- Available as 1023 pin Hi-CTE flip chip ceramic land grid (FC-CLGA) and ceramic ball grid array (FC-CBGA)

3. Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the PC8641. The PC8641 is currently targeted to these specifications.

3.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

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3.1.1 Absolute Maximum Ratings

Table 3-1 provides the absolute maximum ratings.

Table 3-1. Absolute Maximum Ratings⁽¹⁾

Characteristic	Symbol	Maximum Value	Unit	Notes	
Cores supply voltages	V _{DD-Core0} V _{DD-Core1}	-0.3 to 1.21 V	V	(2)	
Cores PLL supply	AV _{DD-Core0} AV _{DD-Core1}	-0.3 to 1.21 V	V		
SerDes Transceiver Supply (Ports 1 and 2)	SV _{DD}	-0.3 to 1.21 V	V		
SerDes Serial I/O Supply Port 1	XV _{DD-SRDS1}	-0.3 to 1.21 V	V		
SerDes Serial I/O Supply Port 2	XV _{DD-SRDS2}	-0.3 to 1.21 V	V		
SerDes DLL and PLL supply voltage for Port 1 and Port 2	AV _{DD-SRDS1} AV _{DD-SRDS2}	-0.3 to 1.21 V	V		
Platform Supply voltage	V _{DD-PLAT}	-0.3 to 1.21 V	V		
Local Bus and Platform PLL supply voltage	AV _{DD-LB} AV _{DD-PLAT}	-0.3 to 1.21 V	V		
DDR and DDR2 SDRAM I/O supply voltages	D1_GV _{DD}	-0.3 to 2.75 V	V	(3)	
	D2_GV _{DD}	-0.3 to 1.98 V	V	(3)	
eTSEC 1 and 2 I/O supply voltage	LV _{DD}	-0.3 to 3.63 V	V	(4)	
		-0.3 to 2.75 V	V	(4)	
eTSEC 3 and 4 I/O supply voltage	TV _{DD}	-0.3 to 3.63 V	V	(4)	
		-0.3 to 2.75 V	V	(4)	
Local Bus, DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, JTAG, Power management, I ² C, JTAG and Miscellaneous I/O voltage	OV _{DD}	-0.3 to 3.63 V	V		
Input voltage	DDR and DDR2 SDRAM signals	D _n _MV _{IN}	-0.3 to (D _n _GV _{DD} + 0.3)	V	(5)
	DDR and DDR2 SDRAM reference	D _n _MV _{REF}	-0.3 to (D _n _GV _{DD} /2 + 0.3)	V	
	Three-speed Ethernet signals	LV _{IN} TV _{IN}	GND to (LV _{DD} + 0.3) GND to (TV _{DD} + 0.3)	V	(5)
	DUART, Local Bus, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, JTAG, Power management, I ² C, JTAG and Miscellaneous I/O voltage	OV _{IN}	GND to (OV _{DD} + 0.3)	V	(5)
Storage temperature range	T _{STG}	-55 to 150	°C		

- Notes:
- Functional and tested operating conditions are given in Table 3-2 on page 7. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
 - Core 1 characteristics apply only to PC8641D. If two separate power supplies are used for V_{DD-Core0} and V_{DD-Core1}, they must be kept within 100 mV of each other during normal run time.
 - The -0.3 to 2.75V range is for DDR and -0.3 to 1.98V range is for DDR2.
 - The 3.63V maximum is only supported when the port is configured in GMII, MII, RMII, or TBI modes; otherwise the 2.75V maximum applies. See Section 9.2 "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications" on page 27 for details on the recommended operating conditions per protocol.
 - During run time (M,L,T,O)V_{IN} and D_n_MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 3-1 on page 8.

3.1.2 Recommended Operating Conditions

Table 3-2 provides the recommended operating conditions for the PC8641. Note that the values in Table 3-2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed. For details on order information and specific operating conditions for parts, see Section 22. "Ordering Information" on page 106."

Table 3-2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes	
Cores supply voltages	V_{DD_Core0}	$1.10 \pm 50 \text{ mV}$	V	(1)(2)(8)	
	V_{DD_Core1}	$1.05 \pm 50 \text{ mV}$		(1)(2)(7)	
Cores PLL supply	AV_{DD_Core0}	$1.10 \pm 50 \text{ mV}$	V	(8)	
	AV_{DD_Core1}	$1.05 \pm 50 \text{ mV}$		(7)	
SerDes Transceiver Supply (Ports 1 and 2)	SV_{DD}	$1.10 \pm 50 \text{ mV}$	V	(8)(11)	
		$1.05 \pm 50 \text{ mV}$		(7)(11)	
SerDes Serial I/O Supply Port 1	XV_{DD_SRDS1}	$1.10 \pm 50 \text{ mV}$	V	(8)	
		$1.05 \pm 50 \text{ mV}$		(7)	
SerDes Serial I/O Supply Port 2	XV_{DD_SRDS2}	$1.10 \pm 50 \text{ mV}$	V	(8)	
		$1.05 \pm 50 \text{ mV}$		(7)	
SerDes DLL and PLL supply voltage for Port 1 and Port 2	AV_{DD_SRDS1}	$1.10 \pm 50 \text{ mV}$	V	(8)	
	AV_{DD_SRDS2}	$1.05 \pm 50 \text{ mV}$		(7)	
Platform Supply voltage	V_{DD_PLAT}	$1.10 \pm 50 \text{ mV}$	V	(8)	
		$1.05 \pm 50 \text{ mV}$		(7)	
Local Bus and Platform PLL supply voltage	AV_{DD_LB}	$1.10 \pm 50 \text{ mV}$	V	(8)	
	AV_{DD_PLAT}	$1.05 \pm 50 \text{ mV}$		(7)	
DDR and DDR2 SDRAM I/O supply voltages	$D1_GV_{DD}$	$2.5V \pm 125 \text{ mV}$	V	(9)	
	$D2_GV_{DD}$	$1.8V \pm 90 \text{ mV}$		(9)	
eTSEC 1 and 2 I/O supply voltage	LV_{DD}	$3.3V \pm 165 \text{ mV}$	V	(10)	
		$2.5V \pm 125 \text{ mV}$		(10)	
eTSEC 3 and 4 I/O supply voltage	TV_{DD}	$3.3V \pm 165 \text{ mV}$	V	(10)	
		$2.5V \pm 125 \text{ mV}$		(10)	
Local Bus, DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, JTAG, Power management, I ² C, JTAG and Miscellaneous I/O voltage	OV_{DD}	$3.3V \pm 165 \text{ mV}$	V	(5)	
Input voltage	DDR and DDR2 SDRAM signals	Dn_MV_{IN}	GND to Dn_GV_{DD}	V	(3)(6)
	DDR and DDR2 SDRAM reference	Dn_MV_{REF}	$Dn_GV_{DD}/2 \pm 1\%$	V	
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	(4)(6)
	DUART, Local Bus, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, JTAG, Power management, I ² C, JTAG and Miscellaneous I/O voltage	OV_{IN}	GND to OV_{DD}	V	(5)(6)
Operating temperature	T_J T_C	$T_C = -55^\circ \text{C}$ to $T_J = 125^\circ \text{C}$	$^\circ \text{C}$		

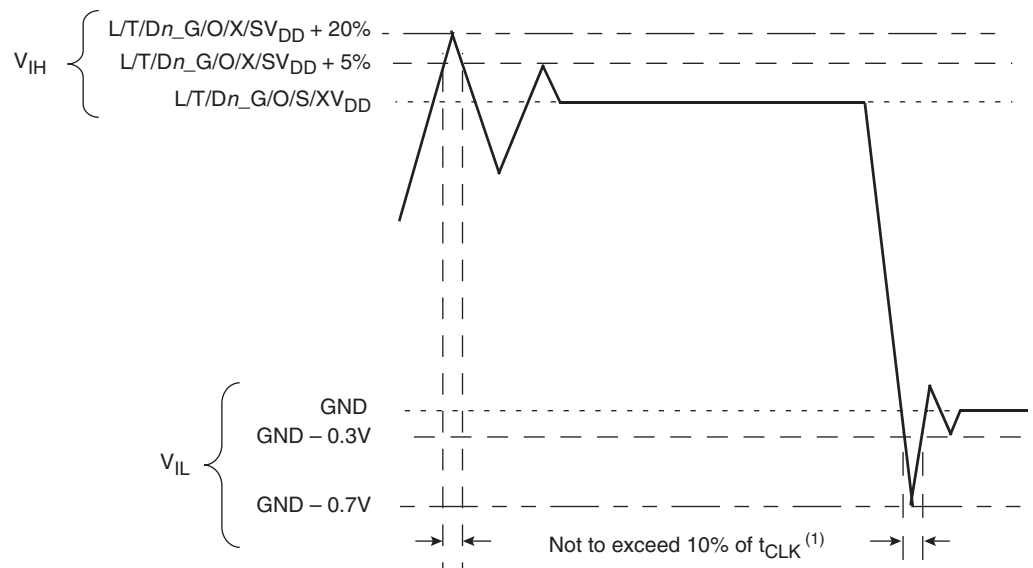
Notes: 1. Core 1 characteristics apply only to PC8641D.

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2. If two separate power supplies are used for V_{DD_Core0} and V_{DD_Core1} , they must be at the same nominal voltage and the individual power supplies must be tracked and kept within 100 mV of each other during normal run time.
3. **Caution:** Dn_MV_{IN} must meet the overshoot/undershoot requirements for Dn_GV_{DD} as shown in Figure 3-1.
4. **Caution:** L/TV_{IN} must meet the overshoot/undershoot requirements for L/TV_{DD} as shown in Figure 3-1 during regular run time.
5. **Caution:** OV_{IN} must meet the overshoot/undershoot requirements for OV_{DD} as shown in Figure 3-1 during regular run time.
6. Timing limitations for $M,L,T,O)V_{IN}$ and Dn_MV_{REF} during regular run time is provided in Figure 3-1.
7. Applies to a core frequency of 1333 MHz and below.
8. Applies to a core frequency above 1333 MHz.
9. The $2.5V \pm 125\text{ mV}$ range is for DDR and $1.8V \pm 90\text{ mV}$ range is for DDR2.
10. See Section 9.2 "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications" on page 27 for details on the recommended operating conditions per protocol.
11. The PCI Express interface of the device is expected to receive signals from 0.175 to 1.2V. For more information refer to Section 15.4.3 "Differential Receiver (RX) Input Specifications" on page 59.

Figure 3-1 shows the undershoot and overshoot voltages at the interfaces of the PC8641.

Figure 3-1. Overshoot/Undershoot Voltage for $Dn_GV_{DD}/OV_{DD}/LV_{DD}$



Note: 1. t_{CLK} references clocks for various functional blocks as follows:

DDR n = 10% of Dn_MCK period

eTsec n = 10% of ECn_GTX_CLK125 period

Local Bus = 10% of $LCLK[0:2]$ period

SerDes = 10% of SDn_REF_CLK period

I²C = 10% of $SYSCLK$

JTAG = 10% of $SYSCLK$

The PC8641 core voltage must always be provided at nominal V_{DD_Core} (See [Table 3-2 on page 7](#) for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in [Table 3-2](#). The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and L/TV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced to each externally supplied Dn_MV_{REF} signal (nominally set to $Dn_GV_{DD}/2$) as is appropriate for the (SSTL-18 and SSTL-25) electrical signaling standards.

3.1.3 Output Driver Characteristics

[Table 3-3](#) provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3-3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
DDR1 signal	18 36 (half strength mode)	$Dn_GV_{DD} = 2.5V$	(4)(9)
DDR2 signal	18 36 (half strength mode)	$Dn_GV_{DD} = 1.8V$	(1)(5)(9)
Local Bus signals	45 25	$OV_{DD} = 3.3V$	(2)(6)
eTSEC/10/100 signals	45	$T/LV_{DD} = 3.3V$	(6)
	30	$T/LV_{DD} = 2.5V$	(6)
DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, JTAG, Power management, JTAG and Miscellaneous I/O voltage	45	$OV_{DD} = 3.3V$	(6)
I ² C	150	$OV_{DD} = 3.3V$	(7)
SRIO, PCI Express	100	$SV_{DD} = 1.1/1.05V$	(3)(8)

- Notes:
1. See the DDR Control Driver registers in the PC8641D reference manual for more information.
 2. Only the following local bus signals have programmable drive strengths: LALE, LAD[0:31], LDP[0:3], LA[27:31], LCKE, LCS[1:2], LWE[0:3], LGPL1, LGPL2, LGPL3, LGPL4, LGPL5, LCLK[0:2]. The other local bus signals have a fixed drive strength of 45 Ω . See the POR Impedance Control register in the PC8641D reference manual for more information about local bus signals and their drive strength programmability.
 3. See [Section 18. "Signal Listings" on page 75](#) for details on resistor requirements for the calibration of $SDn_IMP_CAL_TX$ and $SDn_IMP_CAL_RX$ transmit and receive signals.
 4. Stub Series Terminated Logic (SSTL-25) type pins.
 5. Stub Series Terminated Logic (SSTL-18) type pins.
 6. Low Voltage Transistor-Transistor Logic (LVTTL) type pins.
 7. Open Drain type pins.
 8. Low Voltage Differential Signaling (LVDS) type pins.
 9. The drive strength of the DDR interface in half strength mode is at $T_J = 105C$ and at Dn_GV_{DD} (min).

3.2 Power Up/Down Sequence

The PC8641 requires its power rails to be applied in a specific sequence in order to ensure proper device operation.

Note: The recommended maximum ramp up time for power supplies is 20 milliseconds.

The chronological order of power up is:

1. All power rails other than DDR I/O (Dn_GV_{DD} , and Dn_MV_{REF}).

Note: There is no required order sequence between the individual rails for this item (# 1). However, V_{DD_PLAT} , AV_{DD_PLAT} rails must reach 90% of their recommended value before the rail for Dn_GV_{DD} , and Dn_MV_{REF} (in next step) reaches 10% of their recommended value. AV_{DD} type supplies must be delayed with respect to their source supplies by the RC time constant of the PLL filter circuit described in [Section 21.2.1 "PLL Power Supply Filtering"](#) on page 96.

2. Dn_GV_{DD} , Dn_MV_{REF}

Note: It is possible to leave the related power supply (Dn_GV_{DD} , Dn_MV_{REF}) turned off at reset for a DDR port that will not be used. Note that these power supplies can only be powered up again at reset for functionality to occur on the DDR port.

3. SYSCLK

The recommended order of power down is as follows:

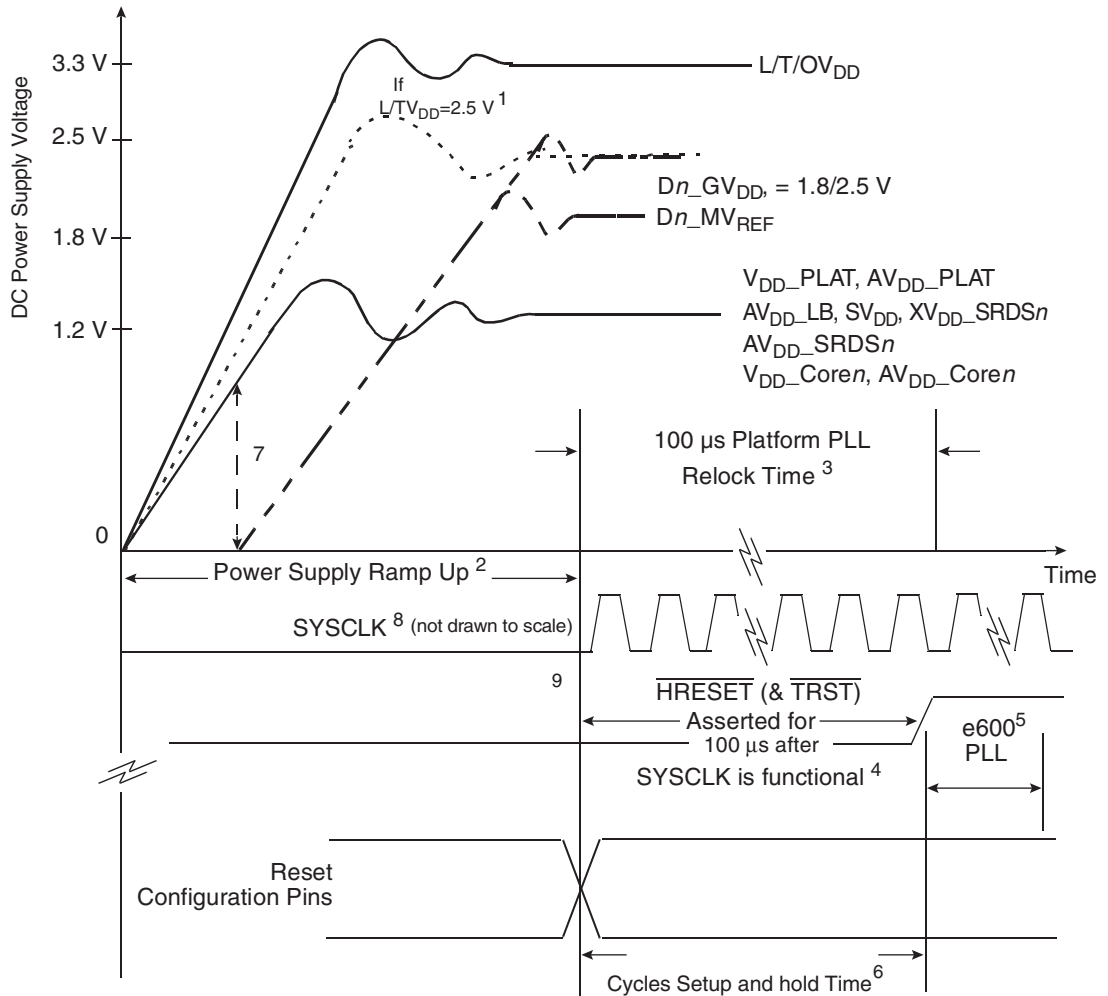
1. Dn_GV_{DD} , Dn_MV_{REF}
2. All power rails other than DDR I/O (Dn_GV_{DD} , Dn_MV_{REF}).

Note: SYSCLK may be powered down simultaneous to either of item # 1 or # 2 in the power down sequence. Beyond this, the power supplies may power down simultaneously if the preservation of DDRn memory is not a concern.

See [Figure 3-2 on page 11](#) for more details on the Power and Reset Sequencing details.

Figure 3-2 illustrates the Power Up sequence as described above.

Figure 3-2. PC8641 Power-Up and Reset Sequence



- Notes:
1. Dotted waveforms correspond to optional supply values for a specified power supply. See [Table 3-2 on page 7](#).
 2. The recommended maximum ramp up time for power supplies is 20 milliseconds.
 3. Refer to [Section 6. "RESET Initialization" on page 17](#) for additional information on PLL relock and reset signal assertion timing requirements.
 4. Refer to [Table 6-1 on page 17](#) for additional information on reset configuration pin setup timing requirements. In addition see [Figure 21-6 on page 104](#) regarding HRESET and JTAG connection details including TRST.
 5. e600 PLL relock time is 100 microseconds maximum plus 255 MPX_clk cycles.
 6. POR configuration signals must be driven on reset. See [Section 6. "RESET Initialization" on page 17](#) for more information on setup and hold time of reset configuration signals.
 7. V_{DD}_PLAT, AV_{DD}_PLAT must strictly reach 90% of their recommended voltage before the rail for D_n_GV_{DD}, and D_n_MV_{REF} reaches 10% of their recommended voltage.
 8. SYSCLK must be driven only AFTER the power for the various power supplies is stable.
 9. In device sleep mode, the reset configuration signals for DRAM types (TSEC2_TXD[4], TSEC2_TX_ER) must be valid BEFORE HRESET is asserted.

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4. Power Characteristics

The power dissipation for the dual core PC8641D device is shown in [Table 4-1](#).

Table 4-1. PC8641D Power Dissipation (Dual Core)

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	V _{DD_Coren} , V _{DD_PLAT} (Volts)	Junction Temperature	Power (Watts)	Notes
Typical	1500 MHz	600 MHz	1.1V	65° C	32.1	(1)(2)
Thermal				105° C	43.4	(1)(3)(5)
Maximum				110° C	49.9	(1)(4)(5)
				125° C	TBC	(1)(4)(5)
Typical	1333 MHz	533 MHz	1.05V	65° C	23.9	(1)(2)
Thermal				105° C	30	(1)(3)(5)
Maximum				110° C	34.1	(1)(4)(5)
				125° C	TBC	(1)(4)
Typical	1250 MHz	500 MHz	1.05V	65° C	23.9	(1)(2)
Thermal				105° C	30	(1)(3)
Maximum				110° C	34.1	(1)(4)
				125° C	TBC	(1)(4)
Typical	1000 MHz	400 MHz	1.05V	65° C	23.9	(1)(2)
Thermal				105° C	30	(1)(3)
Maximum				110° C	34.1	(1)(4)
				125° C	TBC	(1)(4)
Typical	1000 MHz	500 MHz	0.95V 1.05V	65° C	16.2	(1)(2)(5)
Thermal				105° C	21.8	(1)(3)(5)
Maximum				110° C	25	(1)(4)(5)
				125° C	TBC	(1)(4)(5)

- Notes:
1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
 2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD_Coren}) and 65° C junction temperature (see [Table 3-2 on page 7](#)) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz with one core at 100% efficiency and the second core at 65% efficiency.
 3. Thermal power is the average power measured at nominal core voltage (V_{DD_Coren}) and maximum operating junction temperature (see [Table 3-2](#)) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz on both cores and a typical workload on platform interfaces.
 4. Maximum power is the maximum power measured at nominal core voltage (V_{DD_Coren}) and maximum operating junction temperature (see [Table 3-2](#)) while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep all the execution units maximally busy on both cores.
 5. These power numbers are for Part Number PC8641Dxx1000NX only. V_{DD_Coren} = 0.95V and V_{DD_PLAT} = 1.05V.

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The power dissipation for the PC8641 single core is shown in [Table 4-2](#).

Table 4-2. PC8641D Individual Supply Maximum Power Dissipation⁽¹⁾

Component Description	Supply Voltage (Volts)	Power (Watts)	Notes
Per Core voltage Supply	$V_{DD_Core0}/V_{DD_Core1} = 1.1V$ at 1500 MHz	21.00	
Per Core PLL voltage supply	$AV_{DD_Core0}/AV_{DD_Core1} = 1.1V$ at 1500 MHz	0.13	
Per Core voltage Supply	$V_{DD_Core0}/V_{DD_Core1} = 1.05V$ at 1333 MHz	17.00	
Per Core PLL voltage supply	$AV_{DD_Core0}/AV_{DD_Core1} = 1.05V$ at 1333 MHz	0.13	
Per Core voltage Supply	$V_{DD_Core0}/V_{DD_Core1} = 0.95V$ at 1000 MHz	11.50	(5)
Per Core PLL voltage supply	$AV_{DD_Core0}/AV_{DD_Core1} = 0.95V$ at 1000 MHz	0.13	(5)
DDR Controller I/O voltage supply	$Dn_GV_{DD} = 2.5V$ at 400 MHz	0.80	(2)
	$Dn_GV_{DD} = 1.8V$ at 533 MHz	0.68	(2)
	$Dn_GV_{DD} = 1.8V$ at 600 MHz	0.77	(2)
16-bit FIFO at 200 MHz eTsec 1&2/3&4 Voltage Supply	$L/TV_{DD} = 3.3V$	0.11	(2)(3)
non-FIFO eTsec Voltage Supply	$L/TV_{DD} = 3.3V$	0.08	(2)
x8 SerDes transceiver Supply	$SV_{DD} = 1.1V$	0.70	(2)
x8 SerDes I/O Supply	$XV_{DD_SRDSn} = 1.1V$	0.66	(2)
SerDes PLL voltage supply Port 1 or 2	$AV_{DD_SRDS1}/AV_{DD_SRDS2} = 1.1V$	0.10	
Platform I/O Supply	$OV_{DD} = 3.3V$	0.45	(4)
Platform source Supply	$V_{DD_PLAT} = 1.1V$ at 600 MHz	12.00	
Platform source Supply	$V_{DD_PLAT} = 1.05 Vn$ at 500 MHz	9.80	(5)
Platform source Supply	$V_{DD_PLAT} = 1.05 Vn$ at 400 MHz	7.70	
Platform, Local Bus PLL voltage Supply	$AV_{DD_PLAT}, AV_{DD_LB} = 1.1V$	0.10	

- Notes:
1. This is a maximum power supply number which is provided for power supply and board design information. The numbers are based on 100% bus utilization for each component. The components listed are not expected to have 100% bus usage simultaneously for all components. Actual numbers may vary based on activity.
 2. Number is based on a per port/interface value.
 3. This is based on one eTSEC port used. Since 16-bit FIFO mode involves two ports, the number will need to be multiplied by two for the total. The other eTSEC protocols dissipate less than this number per port. Note that the power needs to be multiplied by the number of ports used for the protocol for the total eTSEC port power dissipation.
 4. This includes Local Bus, DUART, JTAG, I²C, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, JTAG and Miscellaneous I/O voltage.
 5. These power numbers are for Part Number PC8641xxx1000NX only. $V_{DD_Coren} = 0.95V$ and $V_{DD_PLAT} = 1.05V$.

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The estimated power dissipation for the PC8641 single core device is shown in [Table 4-3](#). The listed next to each number is to indicate that the number is based on an estimate.

Table 4-3. PC8641 Power Dissipation (Single Core)

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	V_{DD_Coren} , V_{DD_PLAT} (Volts)	Junction Temperature	Power (Watts)	Notes
Typical	1333 MHz	533 MHz	1.05V	65° C	16.3	(1)(2)
Thermal				105° C	20.2	(1)(3)
Maximum				110° C	23.2	(1)(4)
				125° C	TBC	(1)(4)
Typical	1250 MHz	500 MHz	1.05V	65° C	16.3	(1)(2)
Thermal				105° C	20.2	(1)(3)
Maximum				110° C	23.2	(1)(4)
				125° C	TBC	(1)(4)
Typical	1000 MHz	400 MHz	1.05V	65° C	16.3	(1)(2)
Thermal				105° C	20.2	(1)(3)
Maximum				110° C	23.2	(1)(4)
				125° C	TBC	(1)(4)
Typical	1000 MHz	500 MHz	0.95V	65° C	11.6	(1)(2)(5)
Thermal				105° C	14.4	(1)(3)(5)
Maximum			1.05V	110° C	16.5	(1)(4)(5)
				125° C	TBC	(1)(4)(5)

- Notes:
1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
 2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD_Coren}) and 65° C junction temperature (see [Table 3-2 on page 7](#)) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz.
 3. Thermal power is the average power measured at nominal core voltage (V_{DD_Coren}) and maximum operating junction temperature (see [Table 3-2](#)) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz and a typical workload on platform interfaces.
 4. Maximum power is the maximum power measured at nominal core voltage (V_{DD_Coren}) and maximum operating junction temperature (see [Table 3-2](#)) while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep all the execution units maximally busy.
 5. These power numbers are for Part Number PC8641xx1000NX only. $V_{DD_Coren} = 0.95V$ and $V_{DD_PLAT} = 1.05V$.

5. Input Clocks

Table 5-1 provides the system clock (SYSCLK) DC specifications for the PC8641.

Table 5-1. SYSCLK DC Electrical Characteristics ($OV_{DD} = 3.3V \pm 165\text{ mV}$)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current ($V_{IN}^{(1)} = 0V$ or $V_{IN} = V_{DD}$)	I_{IN}	–	± 5	μA

Note: 1. Note that the symbol OV_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 3-1 on page 6 and Table 3-2 on page 7.

5.1 System Clock Timing

Table 5-2 provides the system clock (SYSCLK) AC timing specifications for the PC8641.

Table 5-2. SYSCLK AC Timing Specifications
(At Recommended Operating Conditions with $OV_{DD} = 3.3V \pm 165\text{ mV}$. See Table 3-2 on page 7)

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	66	–	166.66	MHz	(1)
SYSCLK cycle time	t_{SYSCLK}	6	–	–	ns	–
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	(2)
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	–	60	%	(3)
SYSCLK jitter	–	–	–	150	ps	(4)(5)

Notes: 1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2 "MPX to SYSCLK PLL Ratio" on page 87 and Section 19.3 "e600 to MPX clock PLL Ratio" on page 88, for ratio settings.

2. Rise and fall times for SYSCLK are measured at 0.4V and 2.7V.

3. Timing is guaranteed by design and characterization.

4. This represents the total input jitter: short term and long term, and is guaranteed by design.

5. The SYSCLK driver's closed loop jitter bandwidth should be < 500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter. Note that the frequency modulation for SYSCLK reduces significantly for the spread spectrum source case. This is to guarantee what is supported based on design.

5.1.1 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 5-3 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the PC8641 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate con-

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cerns, and the PC8641 is compatible with spread spectrum sources if the recommendations listed in [Table 5-3](#) are observed.

Table 5-3. Spread Spectrum Clock Source Recommendations
(At Recommended Operating Conditions. See [Table 3-2 on page 7](#))

Parameter	Min	Max	Unit	Notes
Frequency modulation	–	50	kHz	(1)
Frequency spread	–	1.0	%	(1)(2)

- Notes:
1. Guaranteed by design.
 2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in [Table 5-3](#).

It is imperative to note that the processor’s minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e600 core frequency should avoid violating the stated limits by using down-spreading only.

$\overline{SDn_REF_CLK}$ and $\overline{SDn_REF_CLK}$ was designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30-33kHz rate is allowed), assuming both ends have same reference clock. For better results use a source without significant unintended modulation.

5.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (MPX clock). The output of the sampling latch is then used as an input to the counters of the PIC. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the MPX clock. That is, minimum clock high time is $2 \times t_{MPX}$, and minimum clock low time is $2 \times t_{MPX}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

5.3 eTSEC Gigabit Reference Clock Timing

[Table 5-4](#) provides the eTSEC gigabit reference clocks (EC_1_GTX_CLK125 and EC_2_GTX_CLK125) AC timing specifications for the PC8641.

Table 5-4. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
ECn_GTX_CLK125 frequency	f_{G125}	–	125	–	MHz	
ECn_GTX_CLK125 cycle time	t_{G125}	–	8	–	ns	
EC_GTX_CLK125 duty cycle - GMII, TBI - 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	45 47	–	55 53	%	(1)(2)

- Notes:
1. Timing is guaranteed by design and characterization.
 2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See [Section 9.2.6 "RGMII and RTBI AC Timing Specifications" on page 36](#) for duty cycle for 10Base-T and 100Base-T reference clock.

Note: The phase between the output clocks TSEC1_GTX_CLK and TSEC2_GTX_CLK (ports 1 and 2) is no more than 100 ps. The phase between the output clocks TSEC3_GTX_CLK and TSEC4_GTX_CLK (ports 3 and 4) is no more than 100 ps.

5.4 Platform Frequency Requirements for PCI-Express and Serial RapidIO

The MPX platform clock frequency must be considered for proper operation of the high-speed PCI Express and Serial RapidIO interfaces as described below.

For proper PCI Express operation, the MPX clock frequency must be greater than or equal to:

$$\frac{527 \text{ MHz} \times (\text{PCI-Express link width})}{16 / (1 + \text{cfg_plat_freq})}$$

Note that at MPX = 400 MHz, $\text{cfg_plat_freq} = 0$ and at MPX > 400 MHz, $\text{cfg_plat_freq} = 1$. Therefore, when operating PCI Express in x8 link width, the MPX platform frequency must be 400 MHz with $\text{cfg_plat_freq} = 0$ or greater than or equal to 527 MHz with $\text{cfg_plat_freq} = 1$.

For proper Serial RapidIO operation, the MPX clock frequency must be greater than:

$$\frac{2 \times (0.80) \times (\text{Serial RapidIO interface frequency}) \times (\text{Serial RapidIO link width})}{64}$$

5.5 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

6. RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the PC8641. [Table 6-1](#) provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 6-1. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	–	µs	
Minimum assertion time for $\overline{\text{SRESET_0}}$ & $\overline{\text{SRESET_1}}$	3	–	SYSClKs	(1)
Platform PLL input setup time with stable SYSClK before $\overline{\text{HRESET}}$ negation	100	–	µs	(2)
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	–	SYSClKs	(1)
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	–	SYSClKs	(1)
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	–	5	SYSClKs	(1)

- Notes:
1. SYSClK is the primary clock input for the PC8641.
 2. This is related to $\overline{\text{HRESET}}$ assertion time. Stable PLL configuration inputs are required when a stable SYSClK is applied. See the PC8641D Integrated Host Processor Reference Manual for more details on the power-on reset sequence.

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Table 6-2 provides the PLL lock times.

Table 6-2. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
(Platform and e600) PLL lock times	–	100	μs	(1)
Local bus PLL	–	50	μs	

Note: 1. The PLL lock time for e600 PLLs require an additional 255 MPX_CLK cycles.

7. DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the PC8641. Note that DDR SDRAM is $Dn_GV_{DD}(typ) = 2.5V$ and DDR2 SDRAM is $Dn_GV_{DD}(typ) = 1.8V$.

7.1 DDR SDRAM DC Electrical Characteristics

Table 7-1 provides the recommended operating conditions for the DDR SDRAM component(s) of the PC8641 when $Dn_GV_{DD}(typ) = 1.8V$.

Table 7-1. DDR2 SDRAM DC Electrical Characteristics for $Dn_GV_{DD}(typ) = 1.8V$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	Dn_GV_{DD}	1.71	1.89	V	(1)
I/O reference voltage	Dn_MV_{REF}	$0.49 \times Dn_GV_{DD}$	$0.51 \times Dn_GV_{DD}$	V	(2)
I/O termination voltage	V_{TT}	$Dn_MV_{REF} - 0.04$	$Dn_MV_{REF} + 0.04$	V	(3)
Input high voltage	V_{IH}	$Dn_MV_{REF} + 0.125$	$Dn_GV_{DD} + 0.3$	V	
Input low voltage	V_{IL}	-0.3	$Dn_MV_{REF} - 0.125$	V	
Output leakage current	I_{OZ}	-9.9	9.9	μA	(4)
Output high current ($V_{OUT} = 1.420V$)	I_{OH}	-13.4	–	mA	
Output low current ($V_{OUT} = 0.280V$)	I_{OL}	13.4	–	mA	

- Notes:
- Dn_GV_{DD} is expected to be within 50 mV of the DRAM Dn_GV_{DD} at all times.
 - Dn_MV_{REF} is expected to be equal to $0.5 \times Dn_GV_{DD}$, and to track Dn_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on Dn_MV_{REF} may not exceed $\pm 2\%$ of the DC value.
 - V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to Dn_MV_{REF} . This rail should track variations in the DC level of Dn_MV_{REF} .

4. Output leakage is measured with all outputs disabled, $0V \leq V_{OUT} \leq Dn_GV_{DD}$.

Table 7-2 provides the DDR capacitance when $GV_{DD}(\text{typ}) = 1.8V$.

Table 7-2. DDR2 SDRAM Capacitance for $Dn_GV_{DD}(\text{typ}) = 1.8V$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, \overline{DQS}	C_{IO}	6	8	pF	(1)
Delta input/output capacitance: DQ, DQS, \overline{DQS}	C_{DIO}	–	0.5	pF	(1)

Note: 1. This parameter is sampled. $Dn_GV_{DD} = 1.8V \pm 0.090V$, $f = 1 \text{ MHz}$, $T_A = 25^\circ \text{C}$, $V_{OUT} = Dn_GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2V.

Table 7-3 provides the recommended operating conditions for the DDR SDRAM component(s) when $Dn_GV_{DD}(\text{typ}) = 2.5V$.

Table 7-3. DDR SDRAM DC Electrical Characteristics for $Dn_GV_{DD}(\text{typ}) = 2.5V$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	Dn_GV_{DD}	2.375	2.625	V	(1)
I/O reference voltage	Dn_MV_{REF}	$0.49 \times Dn_GV_{DD}$	$0.51 \times Dn_GV_{DD}$	V	(2)
I/O termination voltage	V_{TT}	$Dn_MV_{REF} - 0.04$	$Dn_MV_{REF} + 0.04$	V	(3)
Input high voltage	V_{IH}	$Dn_MV_{REF} + 0.15$	$Dn_GV_{DD} + 0.3$	V	
Input low voltage	V_{IL}	-0.3	$Dn_MV_{REF} - 0.15$	V	
Output leakage current	I_{OZ}	-9.9	9.9	μA	(4)
Output high current ($V_{OUT} = 1.95V$)	I_{OH}	-16.2	–	mA	
Output low current ($V_{OUT} = 0.35V$)	I_{OL}	16.2	–	mA	

Notes: 1. Dn_GV_{DD} is expected to be within 50 mV of the DRAM Dn_GV_{DD} at all times.
 2. MV_{REF} is expected to be equal to $0.5 \times Dn_GV_{DD}$, and to track Dn_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on Dn_MV_{REF} may not exceed $\pm 2\%$ of the DC value.
 3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to Dn_MV_{REF} . This rail should track variations in the DC level of Dn_MV_{REF} .
 4. Output leakage is measured with all outputs disabled, $0V \leq V_{OUT} \leq GV_{DD}$.

Table 7-4 provides the DDR capacitance when $Dn_GV_{DD}(\text{typ}) = 2.5V$.

Table 7-4. DDR SDRAM Capacitance for $Dn_GV_{DD}(\text{typ}) = 2.5V$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	(1)
Delta input/output capacitance: DQ, DQS	C_{DIO}	–	0.5	pF	(1)

Note: 1. This parameter is sampled. $Dn_GV_{DD} = 2.5V \pm 0.125V$, $f = 1 \text{ MHz}$, $T_A = 25^\circ \text{C}$, $V_{OUT} = Dn_GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2V.

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Table 7-5 provides the current draw characteristics for MV_{REF} .

Table 7-5. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	–	500	μA	(1)

Note: 1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

7.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

7.2.1 DDR SDRAM Input AC Timing Specifications

Table 7-6 provides the input AC timing specifications for the DDR SDRAM when $Dn_GV_{DD}(typ) = 1.8V$.

Table 7-6. DDR2 SDRAM Input AC Timing Specifications for 1.8V Interface (At Recommended Operating Conditions)

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	–	$Dn_MV_{REF} - 0.25$	V
AC input high voltage	V_{IH}	$Dn_MV_{REF} + 0.25$		V

Table 7-7 provides the input AC timing specifications for the DDR SDRAM when $Dn_GV_{DD}(typ) = 2.5V$.

Table 7-7. DDR SDRAM Input AC Timing Specifications for 2.5V Interface (At Recommended Operating Conditions)

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	–	$Dn_MV_{REF} - 0.31$	V
AC input high voltage	V_{IH}	$Dn_MV_{REF} + 0.31$		V

Table 7-8 provides the input AC timing specifications for the DDR SDRAM interface.

Table 7-8. DDR SDRAM Input AC Timing Specifications (At Recommended Operating Conditions)

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS-MDQ/MECC	t_{CISKEW}			ps	(1)(2)

Table 7-8. DDR SDRAM Input AC Timing Specifications (At Recommended Operating Conditions)

Parameter	Symbol	Min	Max	Unit	Notes
600 MHz		-240	240		(3)
533 MHz		-300	300		(3)
400 MHz		-365	365		

- Notes:
1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
 2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW} . This can be determined by the following equation: $t_{DISKEW} = \pm(T/4 - \text{abs}(t_{CISKEW}))$ where T is the clock period and $\text{abs}(t_{CISKEW})$ is the absolute value of t_{CISKEW} .
 3. Maximum DDR1 frequency is 400 MHz.

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7.2.2 DDR SDRAM Output AC Timing Specifications

Table 7-9. DDR SDRAM Output AC Timing Specifications (At Recommended Operating Conditions)

Parameter	Symbol ⁽¹⁾	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/ $\overline{\text{MCK}}$ [n] crossing	t_{MCK}	3	10	ns	(2)
MCK duty cycle		47.5	52.5		(8)
600 MHz	$t_{\text{MCKH}}/t_{\text{MCK}}$	47	53	%	(9)
533 MHz		47	53		(9)
400 MHz					
ADDR/CMD output setup with respect to MCK					(3)
600 MHz	t_{DDKHAS}	1.10	–	ns	(7)
533 MHz		1.48	–		(7)
400 MHz		1.95	–		
ADDR/CMD output hold with respect to MCK					(3)
600 MHz	t_{DDKHAX}	1.10	–	ns	(7)
533 MHz		1.48	–		(7)
400 MHz		1.95	–		
$\overline{\text{MCS}}$ [n] output setup with respect to MCK					(3)
600 MHz	t_{DDKHCS}	1.10	–	ns	(7)
533 MHz		1.48	–		(7)
400 MHz		1.95	–		
$\overline{\text{MCS}}$ [n] output hold with respect to MCK					(3)
600 MHz	t_{DDKHCX}	1.10	–	ns	(7)
533 MHz		1.48	–		(7)
400 MHz		1.95	–		
MCK to MDQS Skew	t_{DDKMH}	-0.6	0.6	ns	(4)
MDQ/MECC/MDM output setup with respect to MDQS					(5)
600 MHz	t_{DDKHDS} t_{DDKLDS}	500	–	ps	(7)
533 MHz		590	–		(7)
400 MHz		700	–		
MDQ/MECC/MDM output hold with respect to MDQS					(5)
600 MHz	t_{DDKHDX} t_{DDKLDX}	500	–	ps	(7)
533 MHz		590	–		(7)
400 MHz		700	–		
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{\text{MCK}} - 0.6$	$-0.5 \times t_{\text{MCK}} + 0.6$	ns	(6)
MDQS epilogue end	t_{DDKHME}	-0.6	0.6	ns	(6)

- Notes:
- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
 - All MCK/ $\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals $\pm 0.1\text{V}$.
 - ADDR/CMD includes all DDR SDRAM output signals except MCK/ $\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.

4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *PC8641 Integrated Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
7. Maximum DDR1 frequency is 400 MHz.
8. Per the JEDEC spec the DDR2 duty cycle at 600 MHz is the average low and high cycle time values that are defined as the average pulse widths calculated across any consecutive 200 pulses. Jitter can sometimes force single low and high cycle times to drift from the average values. $t_{JIT} = \pm 125$ ps.
9. Per the JEDEC spec the DDR2 duty cycle at 400 and 533 MHz is the low and high cycle time values.

Note: For the ADDR/CMD setup and hold specifications in [Table 7-9 on page 22](#), it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

[Figure 7-1](#) shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

Figure 7-1. Timing Diagram for t_{DDKHMH}

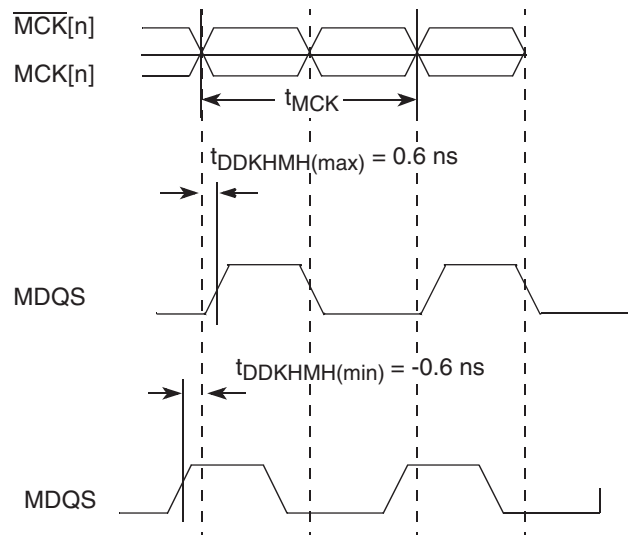


Figure 7-2 shows the DDR SDRAM output timing diagram.

Figure 7-2. DDR SDRAM Output Timing Diagram

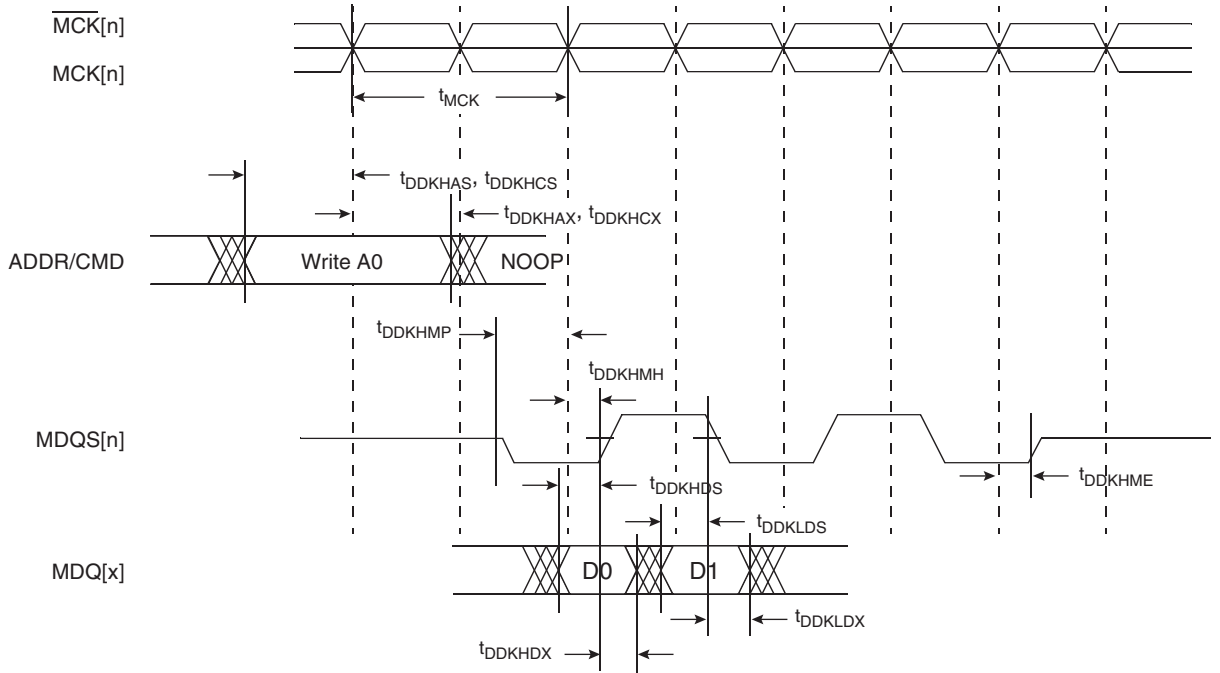
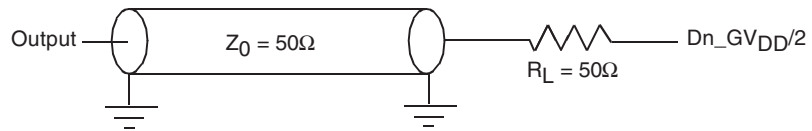


Figure 7-3 provides the AC test load for the DDR bus.

Figure 7-3. DDR AC Test Load



8. DUART

This section describes the DC and AC electrical specifications for the DUART interface of the PC8641.

8.1 DUART DC Electrical Characteristics

Table 8-1 provides the DC electrical characteristics for the DUART interface.

Table 8-1. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current ($V_{IN}^{(1)} = 0V$ or $V_{IN} = V_{DD}$)	I_{IN}	-	± 5	μA
High-level output voltage ($OV_{DD} = mn$, $I_{OH} = -100 \mu A$)	V_{OH}	$OV_{DD} - 0.2$	-	V
Low-level output voltage ($OV_{DD} = min$, $I_{OL} = 100 \mu A$)	V_{OL}	-	0.2	V

Note: 1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 3-1 on page 6 and Table 3-2 on page 7.

8.2 DUART AC Electrical Specifications

Table 8-2 provides the AC timing parameters for the DUART interface.

Table 8-2. DUART AC Timing specifications

Parameter	Value	Unit	Notes
Minimum baud rate	MPX clock/1,048,576	baud	(1)(2)
Maximum baud rate	MPX clock/16	baud	(1)(3)
Oversample rate	16	-	(1)(4)

Notes: 1. Guaranteed by design.
 2. MPX clock refers to the platform clock.
 3. Actual attainable baud rate will be limited by the latency of interrupt processing.
 4. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

9. Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.

9.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps) – GMII/MII/TBI/ RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5V, while the GMII, MII, RMII and TBI interfaces can be operated at 3.3 or 2.5V. Whether the GMII, MII, or TBI interface is operated at 3.3 or 2.5V, the timing is compliant with the IEEE 802.3 standard. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998). The electrical characteristics for MDIO and MDC are specified in [Section 10. "Ethernet Management Interface Electrical Characteristics" on page 39](#).

9.1.1 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII and RTBI drivers and receivers comply with the DC parametric attributes specified in [Table 9-1](#) and [Table 9-2 on page 27](#). The potential applied to the input of a GMII, MII, TBI, RGMII, RMII or RTBI receiver may exceed the potential of the receiver's power supply (i.e., a GMII driver powered from a 3.6-V supply driving V_{OH} into a GMII receiver powered from a 2.5V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 9-1. GMII, MII, RMII, and TBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3V	V_{DD} V_{TVDD}	3.135	3.465	V	(1)(2)
Output high voltage ($V_{DD}/V_{TVDD} = \text{Min}$, $I_{OH} = -4.0 \text{ mA}$)	V_{OH}	2.40	$V_{DD}/V_{TVDD} + 0.3$	V	
Output low voltage ($V_{DD}/V_{TVDD} = \text{Min}$, $I_{OL} = 4.0 \text{ mA}$)	V_{OL}	GND	0.50	V	
Input high voltage	V_{IH}	1.70	$V_{DD}/V_{TVDD} + 0.3$	V	
Input low voltage	V_{IL}	-0.3	0.90	V	
Input high current ($V_{IN} = V_{DD}$, $V_{IN} = V_{TVDD}$)	I_{IH}	–	40	μA	(1)(2)(3)
Input low current ($V_{IN} = \text{GND}$)	I_{IL}	-600	–	μA	(3)

- Notes:
1. V_{DD} supports eTSECs 1 and 2.
 2. V_{TVDD} supports eTSECs 3 and 4.
 3. The symbol V_{IN} , in this case, represents the V_{LVIN} and V_{TVIN} symbols referenced in [Table 3-1 on page 6](#) and [Table 3-2 on page 7](#).

Table 9-2. GMII, MII, RMII, RGMII, RTBI, TBI and FIFO DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5V	V_{DD} V_{TVDD}	2.375	2.675	V	(1)(2)
Output high voltage ($V_{DD}/V_{TVDD} = \text{Min}$, $I_{OH} = -1.0 \text{ mA}$)	V_{OH}	2	$V_{DD}/V_{TVDD} + 0.3$	V	
Output low voltage ($V_{DD}/V_{TVDD} = \text{Min}$, $I_{OL} = 1.0 \text{ mA}$)	V_{OL}	GND - 0.3	0.40	V	
Input high voltage	V_{IH}	1.70	$V_{DD}/V_{TVDD} + 0.3$	V	
Input low voltage	V_{IL}	-0.3	0.70	V	
Input high current ($V_{IN} = V_{DD}$, $V_{IN} = V_{TVDD}$)	I_{IH}	-	10	μA	(1)(2)(3)
Input low current ($V_{IN} = \text{GND}$)	I_{IL}	-15	-	μA	(3)

- Notes:
1. V_{DD} supports eTSECs 1 and 2.
 2. V_{TVDD} supports eTSECs 3 and 4.
 3. The symbol V_{IN} , in this case, represents the V_{IN} and V_{TVIN} symbols referenced in [Table 3-1 on page 6](#) and [Table 3-2 on page 7](#).

9.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII and RTBI are presented in this section.

9.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSECn's TSECn_TX_CLK, while the receive clock must be applied to pin TSECn_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSECn_GTX_CLK pin (while transmit data appears on TSECn_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSECn_GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information see [Section 19.4.2 "Platform to FIFO restrictions" on page 89](#).

Note: The phase between the output clocks TSEC1_GTX_CLK and TSEC2_GTX_CLK (ports 1 and 2) is no more than 100 ps. The phase between the output clocks TSEC3_GTX_CLK and TSEC4_GTX_CLK (ports 3 and 4) is no more than 100 ps.

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A summary of the FIFO AC specifications appears in [Table 9-3](#) and [Table 9-4](#).

Table 9-3. FIFO Mode Transmit AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Input low voltage at 2.5 OV_{DD}	V_{IL}	–	–	0.7	V
Input high voltage at 2.5 OV_{DD}	V_{IH}	1.9	–	–	V
TX_CLK, GTX_CLK clock period	t_{FIT}	5.0	8.0	100	ns
TX_CLK, GTX_CLK duty cycle	t_{FITH}/t_{FIT}	45	50	55	%
TX_CLK, GTX_CLK peak-to-peak jitter	t_{FITJ}	–	–	250	ps
Rise time TX_CLK (20%–80%)	t_{FITR}	–	–	0.75	ns
Fall time TX_CLK (80%–20%)	t_{FITF}	–	–	0.75	ns
FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK	t_{FITDV}	2.0	–	–	ns
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t_{FITDX}	0.5	–	3.0	ns

Table 9-4. FIFO Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Input low voltage at 2.5 OV_{DD}	V_{IL}	–	–	0.7	V
Input high voltage at 2.5 OV_{DD}	V_{IH}	1.9	–	–	V
RX_CLK clock period	t_{FIR}	5.0	8.0	100	ns
RX_CLK duty cycle	t_{FIRH}/t_{FIR}	45	50	55	%
RX_CLK peak-to-peak jitter	t_{FIRJ}	–	–	250	ps
Rise time RX_CLK (20%–80%)	t_{FIRR}	–	–	0.75	ns
Fall time RX_CLK (80%–20%)	t_{FIRF}	–	–	0.75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{FIRDV}	1.5	–	–	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{FIRDX}	0.5	–	–	ns

Timing diagrams for FIFO appear in [Figure 9-1](#) and [Figure 9-2](#) on page 29.

Figure 9-1. FIFO Transmit AC Timing Diagram

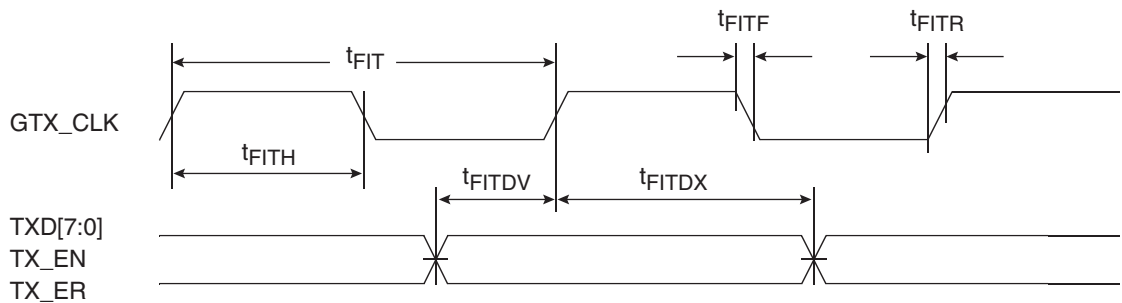
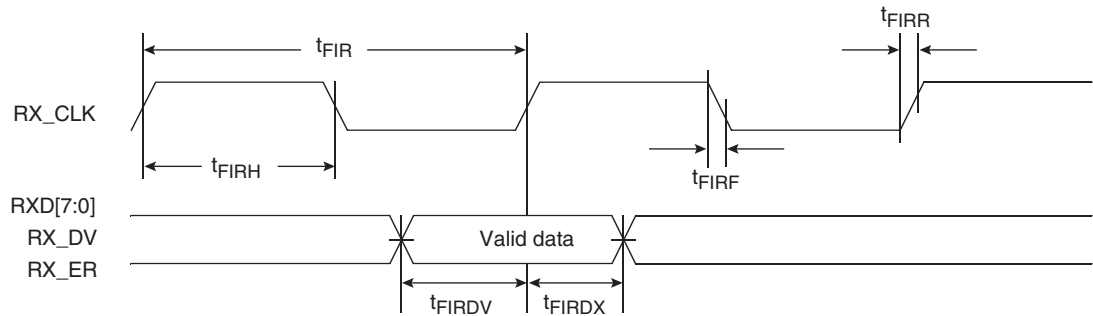


Figure 9-2. FIFO Receive AC Timing Diagram



9.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

9.2.2.1 GMII Transmit AC Timing Specifications

Table 9-5 provides the GMII transmit AC timing specifications.

Table 9-5. GMII Transmit AC Timing Specifications (At Recommended Operating Conditions with L/TV_{DD} of $3.3V \pm 5\%$ and $2.5V \pm 5\%$)

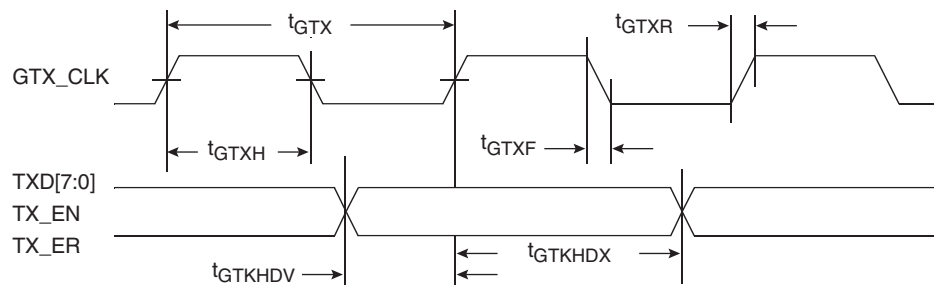
Parameter/Condition	Symbol ⁽¹⁾	Min	Typ	Max	Unit
Input low voltage	V_{IL}	–	–	0.7	V
Input high voltage	V_{IH}	1.9	–	–	V
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	–	–	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	–	5.0	ns
GTX_CLK data clock rise time (20%-80%)	$t_{GTXR}^{(2)}$	–	–	1.0	ns
GTX_CLK data clock fall time (80%-20%)	$t_{GTXF}^{(2)}$	–	–	1.0	ns

Notes: 1. The symbols used for timing specifications herein follow the pattern $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. Guaranteed by design.

Figure 9-3 shows the GMII transmit AC timing diagram.

Figure 9-3. GMII Transmit AC Timing Diagram



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9.2.2.2 GMII Receive AC Timing Specifications

Table 9-6 provides the GMII receive AC timing specifications..

Table 9-6. GMII Receive AC Timing Specifications (At Recommended Operating Conditions with L/TV_{DD} of 3.3V ± 5% and 2.5V ± 5%)

Parameter/Condition	Symbol ⁽¹⁾	Min	Typ	Max	Unit
Input low voltage	V _{IL}	-	-	0.7	V
Input high voltage	V _{IH}	1.9	-	-	V
RX_CLK clock period	t _{GRX}	-	8.0	-	ns
RX_CLK duty cycle	t _{GRXH} /t _{GRX}	40	-	60	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{GRDVKH}	2.0	-	-	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t _{GRDXKH}	0.5	-	-	ns
RX_CLK clock rise (20%-80%)	t _{GRXR} ⁽²⁾	-	-	1.0	ns
RX_CLK clock fall time (80%-20%)	t _{GRXF} ⁽²⁾	-	-	1.0	ns

- Notes: 1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{GRX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low state (L) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 9-4 provides the AC test load for eTSEC.

Figure 9-4. eTSEC AC Test Load

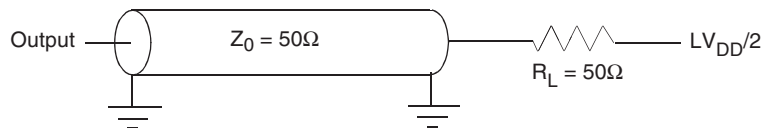
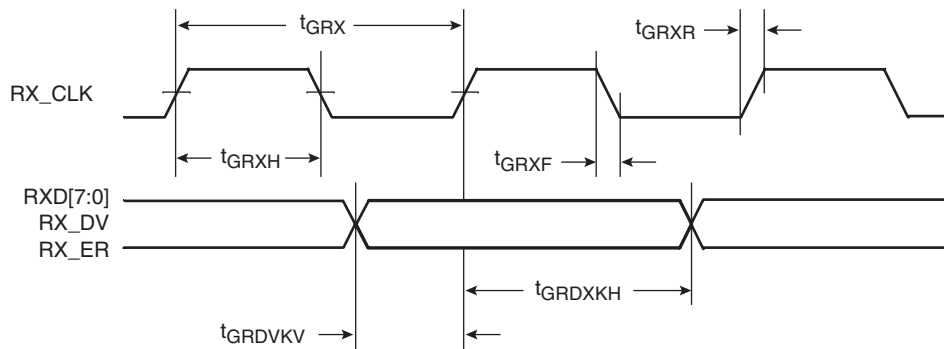


Figure 9-5 shows the GMII receive AC timing diagram.

Figure 9-5. GMII Receive AC Timing Diagram



9.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

9.2.3.1 MII Receive AC Timing Specifications

Table 9-7 provides the MII transmit AC timing specifications.

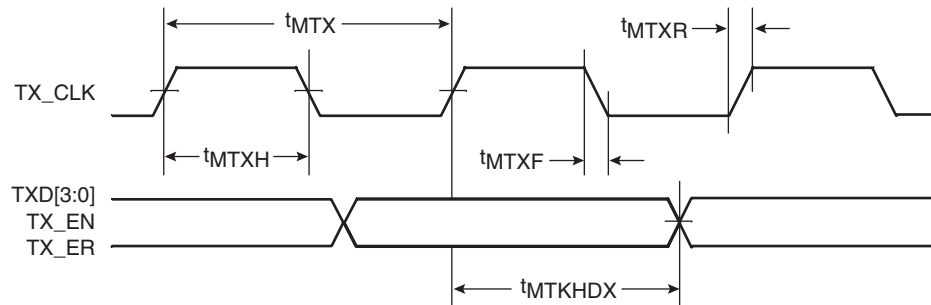
Table 9-7. MII Transmit AC Timing Specifications (At Recommended Operating Conditions with L/TV_{DD} of 3.3V ± 5% and 2.5V ± 5%)

Parameter/Condition	Symbol ⁽¹⁾	Min	Typ	Max	Unit
Input low voltage	V _{IL}	–	–	0.7	V
Input high voltage	V _{IH}	1.9	–	–	V
TX_CLK clock period 10 Mbps	t _{MTX} ⁽²⁾	–	400	–	ns
TX_CLK clock period 100 Mbps	t _{MTX}	–	40	–	ns
TX_CLK duty cycle	t _{MTXH} /t _{MTX}	35	–	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t _{MTKHDX}	1	5	15	ns
TX_CLK data clock rise (20%-80%)	t _{MTXR} ⁽²⁾	1	–	4	ns
TX_CLK data clock fall (80%-20%)	t _{MTXF} ⁽²⁾	1	–	4	ns

- Notes:
- The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
 - Guaranteed by design.

Figure 9-6 shows the MII transmit AC timing diagram.

Figure 9-6. MII Transmit AC Timing Diagram



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9.2.3.2 MII Receive AC Timing Specifications

Table 9-8 provides the MII receive AC timing specifications.

Table 9-8. MII Transmit AC Timing Specifications (At Recommended Operating Conditions with L/TV_{DD} of 3.3V ± 5% and 2.5V ± 5%)

Parameter/Condition	Symbol ⁽¹⁾	Min	Typ	Max	Unit
Input low voltage	V _{IL}	–	–	0.7	V
Input high voltage	V _{IH}	1.9	–	–	V
RX_CLK clock period 10 Mbps	t _{MRX} ⁽²⁾	–	400	–	ns
RX_CLK clock period 100 Mbps	t _{MRX}	–	40	–	ns
RX_CLK duty cycle	t _{MRXH} /t _{MRX}	35	–	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t _{MRDVKH}	10	–	–	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t _{MRDXKH}	10	–	–	ns
RX_CLK clock rise (20%-80%)	t _{MRXR} ⁽²⁾	1	–	4	ns
RX_CLK clock fall time (80%-20%)	t _{MRXF} ⁽²⁾	1	–	4	ns

Notes: 1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. Guaranteed by design.

Figure 9-7 provides the AC test load for eTSEC.

Figure 9-7. eTSEC AC Test Load

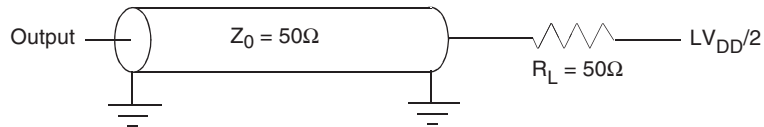
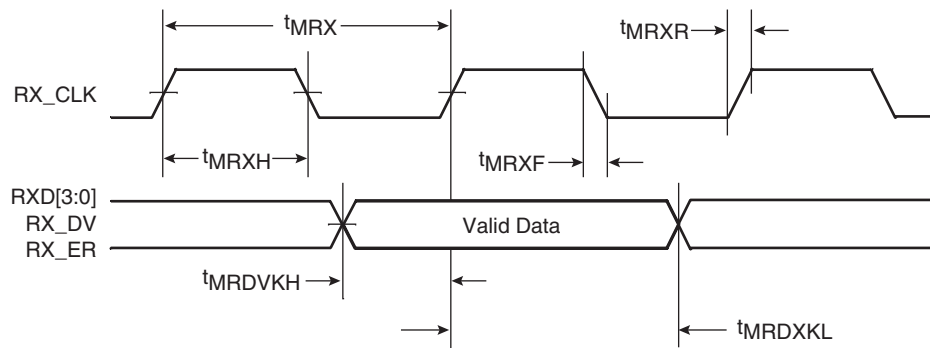


Figure 9-8 shows the MII receive AC timing diagram.

Figure 9-8. MII Receive AC Timing Diagram



9.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

9.2.4.1 TBI Transmit AC Timing Specifications

Table 9-9 provides the TBI transmit AC timing specifications.

Table 9-9. TBI Transmit AC Timing Specifications (At Recommended Operating Conditions with L/TV_{DD} of $3.3V \pm 5\%$ and $2.5V \pm 5\%$)

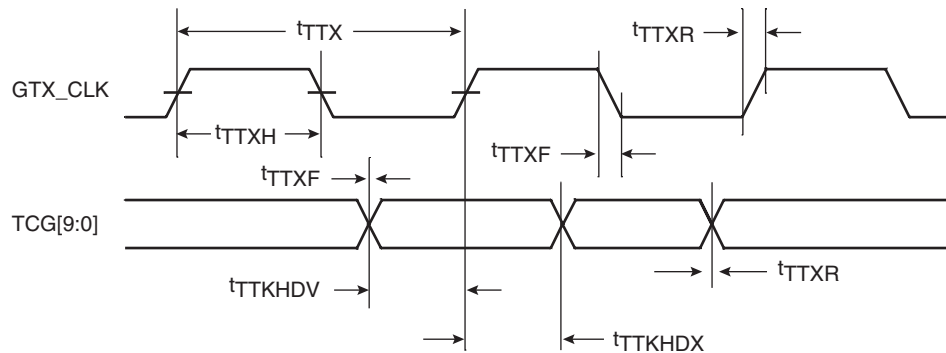
Parameter/Condition	Symbol ⁽¹⁾	Min	Typ	Max	Unit
TCG[9:0] setup time GTX_CLK going high	$t_{TTKH DV}$	2.0	–	–	ns
TCG[9:0] hold time from GTX_CLK going high	$t_{TTKH DX}$	1.0	–	–	ns
GTX_CLK rise (20%–80%)	$t_{TTXR}^{(2)}$	–	–	1.0	ns
GTX_CLK fall time (80%–20%)	$t_{TTXF}^{(2)}$	–	–	1.0	ns

Notes: 1. The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, $t_{TTKH DV}$ symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, $t_{TTKH DX}$ symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. Guaranteed by design.

Figure 9-9 shows the TBI transmit AC timing diagram.

Figure 9-9. TBI Transmit AC Timing Diagram



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9.2.4.2 TBI Receive AC Timing Specifications

Table 9-10 provides the TBI receive AC timing specifications.

Table 9-10. TBI Receive AC Timing Specifications (At Recommended Operating Conditions with L/TV_{DD} of 3.3V ± 5% and 2.5V ± 5%)

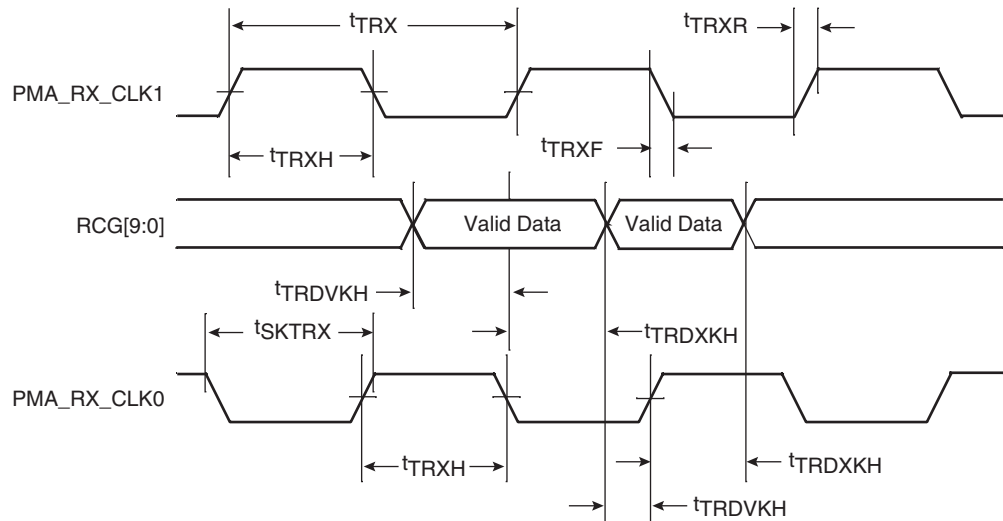
Parameter/Condition	Symbol ⁽¹⁾	Min	Typ	Max	Unit
PMA_RX_CLK[0:1] clock period	t_{TRX}	–	16.0	–	ns
PMA_RX_CLK[0:1] skew	t_{SKTRX}	7.5	–	8.5	ns
PMA_RX_CLK[0:1] duty cycle	t_{TRXH}/t_{TRXF}	40	–	60	%
RCG[9:0] setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	–	–	ns
RCG[9:0] hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.5	–	–	ns
PMA_RX_CLK[0:1] clock rise time (20%-80%)	$t_{TRXR}^{(2)}$	0.7	–	2.4	ns
PMA_RX_CLK[0:1] clock fall time (80%-20%)	$t_{TRXF}^{(2)}$	0.7	–	2.4	ns

Notes: 1. The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).

2. Guaranteed by design.

Figure 9-10 shows the TBI receive AC timing diagram.

Figure 9-10. TBI Receive AC Timing Diagram



9.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when $TBICON[CLKSEL] = 1$ a 125-MHz TBI receive clock is supplied on $TSECn_RX_CLK$ pin (no receive clock is used on $TSECn_TX_CLK$ in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the $TSEC_GTX_CLK125$ pin in all TBI modes.

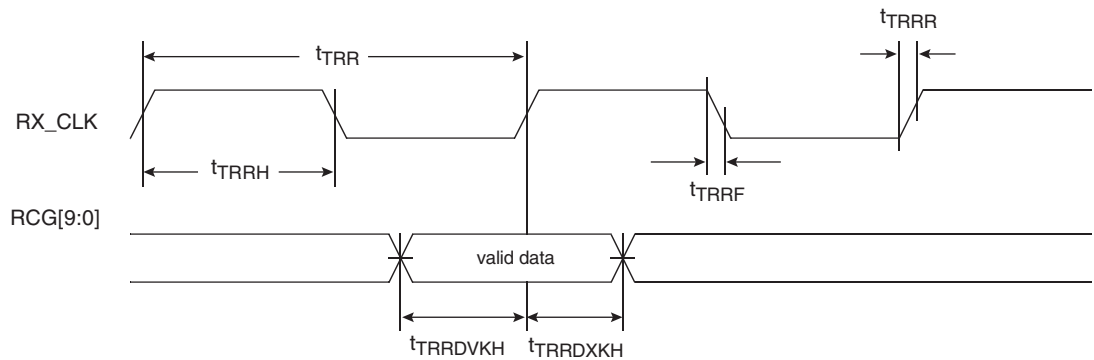
A summary of the single-clock TBI mode AC specifications for receive appears in [Table 9-11](#).

Table 9-11. TBI single-clock Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Input low voltage at 3.3 V_{DD}	V_{IL}	–	–	0.7	V
Input high voltage at 3.3 V_{DD}	V_{IH}	1.9	–	–	V
RX_CLK clock period	t_{TRR}	7.5	8.0	8.5	ns
RX_CLK duty cycle	t_{TRRH}/t_{TRR}	40	50	60	%
RX_CLK peak-to-peak jitter	t_{TRRJ}	–	–	250	ps
Rise time RX_CLK (20%–80%)	t_{TRRH}	–	–	1.0	ns
Fall time RX_CLK (80%–20%)	t_{TRRF}	–	–	1.0	ns
RCG[9:0] setup time to RX_CLK rising edge	$t_{TRRDVKH}$	2.0	–	–	ns
RCG[9:0] hold time to RX_CLK rising edge	$t_{TRRDVKH}$	1.0	–	–	ns

A timing diagram for TBI receive appears in [Figure 9-11](#).

Figure 9-11. TBI Single-Clock Mode Receive AC Timing Diagram



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9.2.6 RGMII and RTBI AC Timing Specifications

Table 9-12 presents the RGMII and RTBI AC timing specifications

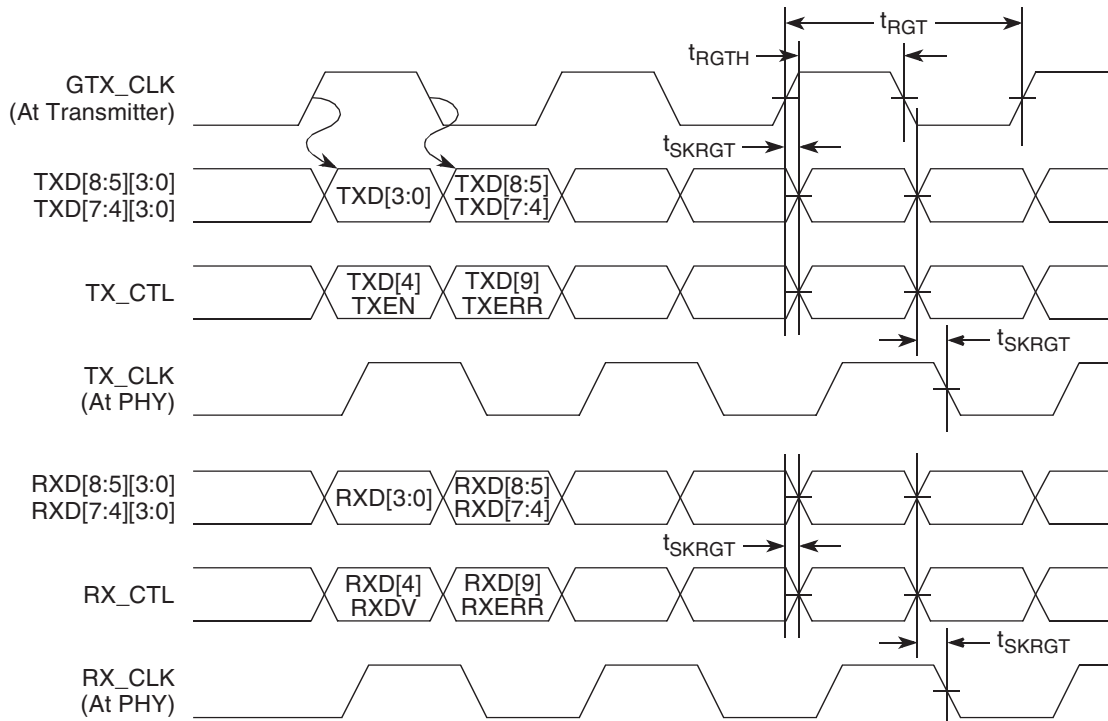
Table 9-12. RGMII and RTBI AC Timing Specifications (At Recommended Operating Conditions with L/TV_{DD} of 2.5V ± 5%)

Parameter/Condition	Symbol ⁽¹⁾	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	$t_{SKRGT}^{(5)}$	-500	0	500	ps
Data to clock input skew (at receiver) ⁽²⁾	t_{SKRGT}	1	–	2.8	ns
Clock period ⁽³⁾	$t_{RGT}^{(5)}$	7.2	8	8.8	ns
Duty cycle for 10BASE-T and 100BASE-TX ⁽³⁾⁽⁴⁾	$t_{RGTH}/t_{RGT}^{(5)}$	40	50	60	%
Rise time (20%-80%)	$t_{RGTR}^{(5)}$	–	–	0.75	ns
Fall time (20%-80%)	$t_{RGTF}^{(5)}$	–	–	0.75	ns

- Notes:
- Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
 - This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
 - For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
 - Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
 - Guaranteed by characterization.

Figure 9-12 shows the RGMII and RTBI AC timing and multiplexing diagrams.

Figure 9-12. RGMII and RTBI AC Timing and Multiplexing Diagrams



9.2.7 RMI AC Timing Specifications

This section describes the RMI transmit and receive AC timing specifications.

9.2.7.1 RMI Transmit AC Timing Specifications

The RMI transmit AC timing specifications are in [Table 9-13](#).

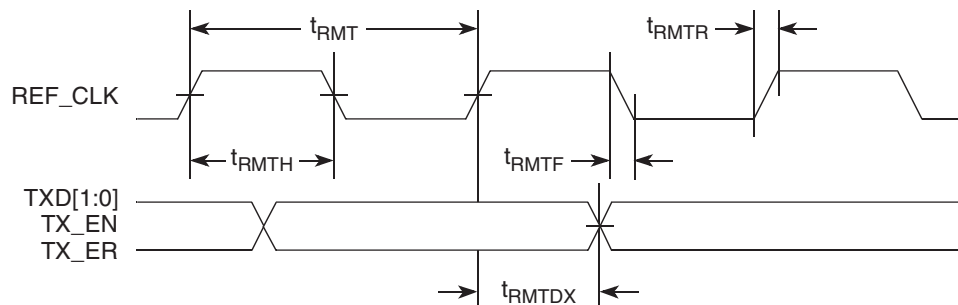
Table 9-13. RMI Transmit AC Timing Specifications (At Recommended Operating Conditions with L/TV_{DD} of $3.3V \pm 5\%$ and $2.5V \pm 5\%$)

Parameter/Condition	Symbol ⁽¹⁾	Min	Typ	Max	Unit
Input low voltage at 3.3 OV_{DD}	V_{IL}	–	–	0.8	V
Input high voltage at 3.3 OV_{DD}	V_{IH}	2.0	–	–	V
REF_CLK clock period	t_{RMT}		20.0		ns
REF_CLK duty cycle	t_{RMTH}/t_{RMT}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMTJ}	–	–	250	ps
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	–	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	–	2.0	ns
REF_CLK to RMI data TXD[1:0], TX_EN delay	t_{RMTDX}	1	–	10	ns

Note: 1. The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(sig- nal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MTKHDX} symbolizes MII in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

[Figure 9-13](#) shows the RMI transmit AC timing diagram.

Figure 9-13. RMI Transmit AC Timing Diagram



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9.2.7.2 RMII Receive AC Timing Specifications

Table 9-14. RMII Receive AC Timing Specifications (At Recommended Operating Conditions with L/TV_{DD} of $3.3V \pm 5\%$ and $2.5V \pm 5\%$)

Parameter/Condition	Symbol ⁽¹⁾	Min	Typ	Max	Unit
Input low voltage at 3.3 OV_{DD}	V_{IL}	–	–	0.8	V
Input high voltage at 3.3 OV_{DD}	V_{IH}	2.0	–	–	V
REF_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMRH}/t_{RMR}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMRJ}	–	–	250	ps
Rise time REF_CLK (20%–80%)	t_{RMRR}	1.0	–	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMRF}	1.0	–	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t_{RMRDV}	4.0	–	–	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t_{RMRDX}	2.0	–	–	ns

Note: 1. The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 9-14 provides the AC test load for eTSEC.

Figure 9-14. eTSEC AC Test Load

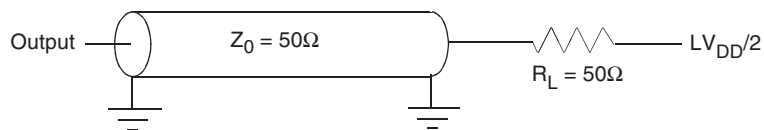
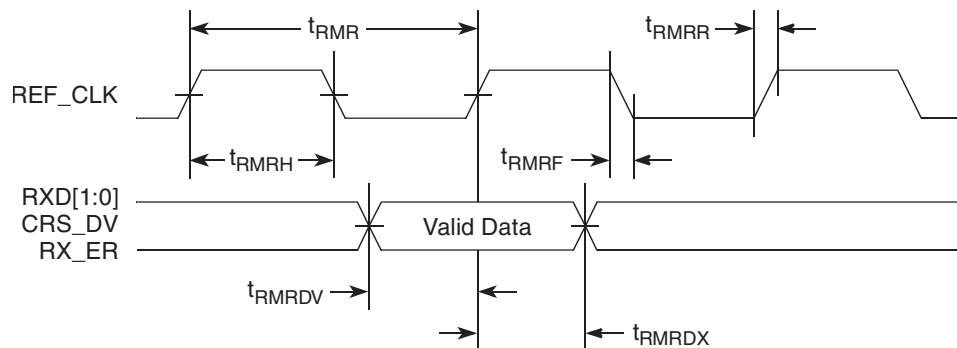


Figure 9-15 shows the RMII receive AC timing diagram.

Figure 9-15. RMII Receive AC Timing Diagram



10. Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI and RTBI are specified in [Section 9. "Ethernet: Enhanced Three-Speed Ethernet \(eTSEC\), MII Management"](#) on page 26.

10.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3V. The DC electrical characteristics for MDIO and MDC are provided in [Table 10-1](#).

Table 10-1. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3V)	OV_{DD}	3.135	3.465	V
Output high voltage ($OV_{DD} = \text{Min}$, $I_{OH} = -1 \text{ mA}$)	V_{OH}	2.10	$OV_{DD} + 0.3$	V
Output low voltage ($OV_{DD} = \text{Min}$, $I_{OL} = 1 \text{ mA}$)	V_{OL}	GND	0.50	V
Input high voltage	V_{IH}	1.70	–	V
Input low voltage	V_{IL}	–	0.90	V
Input high current ($OV_{DD} = \text{Max}$, $V_{IN}^{(1)} = 2.1\text{V}$)	I_{IH}	–	40	μA
Input low current ($OV_{DD} = \text{Max}$, $V_{IN} = 0.5\text{V}$)	I_{IL}	-600	–	μA

Note: 1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in [Table 3-1 on page 6](#) and [Table 3-2 on page 7](#).

10.2 MII Management AC Electrical Specifications

[Table 10-2](#) provides the MII management AC timing specifications.

Table 10-2. MII Management AC Timing Specifications (At Recommended Operating Conditions with OV_{DD} is 3.3V $\pm 5\%$)

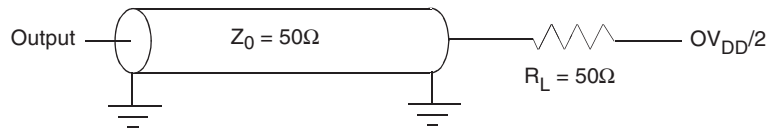
Parameter/Condition	Symbol ⁽¹⁾	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	2.5	–	9.3	MHz	(2)(4)
MDC period	t_{MDC}	80	–	400	ns	
MDC clock pulse width high	t_{MDCH}	32	–	–	ns	
MDC to MDIO valid	t_{MDKHDV}	$2*(t_{MPXCLK} * 8)$	–	–	ns	(5)
MDC to MDIO delay	t_{MDKHDX}	10	–	$2*(t_{MPXCLK} * 8)$	ns	(3)(5)
MDIO to MDC setup time	t_{MDDVKH}	5	–	–	ns	
MDIO to MDC hold time	t_{MDDXKH}	0	–	–	ns	
MDC rise time	t_{MDCR}	–	–	10	ns	(4)
MDC fall time	t_{MDHF}	–	–	10	ns	(4)

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- Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
 2. This parameter is dependent on the system clock speed. (The maximum frequency is the maximum platform frequency divided by 64.)
 3. This parameter is dependent on the system clock speed. (That is, for a system clock of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a system clock of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
 4. Guaranteed by design.
 5. t_{MPXCLK} is the platform (MPX) clock.

Figure 10-1 provides the AC test load for eTSEC.

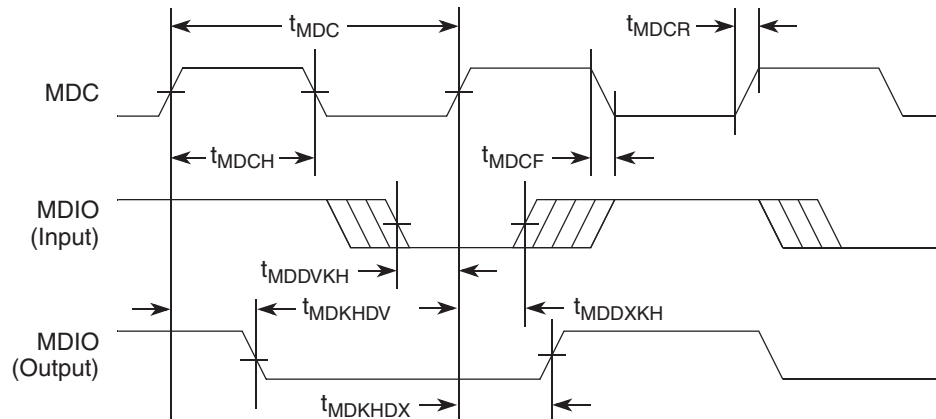
Figure 10-1. eTSEC AC Test Load



Note: Output will see a 50Ω load since what it sees is the transmission line.

Figure 10-2 shows the MII management AC timing diagram.

Figure 10-2. MII Management Interface Timing Diagram



11. Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the PC8641.

11.1 Local Bus DC Electrical Characteristics

Table 11-1 provides the DC electrical characteristics for the local bus interface operating at $OV_{DD} = 3.3V$ DC

Table 11-1. Local Bus DC Electrical Characteristics (3.3V DC)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current ($OV_{IN}^{(1)} = 0V$ or $BV_{IN} = BV_{DD}$)	I_{IN}	–	± 5	μA
High-level output voltage ($OV_{DD} = \text{min}$, $I_{OH} = -2 \text{ mA}$)	V_{OH}	$OV_{DD} - 0.2$	–	V
Low-level output voltage ($OV_{DD} = \text{min}$, $I_{OL} = 2 \text{ mA}$)	V_{OL}	–	0.2	V

Note: 1. Note that the symbol OV_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 3-1 on page 6 and Table 3-2 on page 7.

11.2 Local Bus AC Electrical Specifications

Table 11-2 describes the general timing parameters of the local bus interface at $OV_{DD} = 3.3V$ DC. For information about the frequency range of local bus see Section 19.1 "Clock Ranges" on page 86.

Table 11-2. Local Bus General Timing Parameters ($OV_{DD} = 3.3V$ DC)

Parameter	Configuration	Symbol ⁽¹⁾	Min	Max	Unit	Notes
Local bus cycle time		t_{LBK}	7.5	–	ns	(2)
Local bus duty cycle		t_{LBKH}/t_{LBK}	45	55	%	
LCLK[n] skew to LCLK[m] or LSYNC_OUT		$t_{LBKSKEW}$	–	150	ps	(7)(8)
Input setup to local bus clock (except LUPWAIT)		$t_{LBIVKH1}$	1.8	–	ns	(3)(4)
LUPWAIT input setup to local bus clock		$t_{LBIVKH2}$	1.7	–	ns	(3)(4)
Input hold from local bus clock (except LUPWAIT)		$t_{LBIXKH1}$	1.0	–	ns	(3)(4)
LUPWAIT input hold from local bus clock		$t_{LBIXKH2}$	1.0	–	ns	(3)(4)
LALE output transition to LAD/LDP output transition (LATCH hold time)		t_{LBOTOT}	1.5	–	ns	(6)
Local bus clock to output valid (except LAD/LDP and LALE)		$t_{LBKHOV1}$	–	2.0	ns	
Local bus clock to data valid for LAD/LDP		$t_{LBKHOV2}$	–	2.2	ns	
Local bus clock to address valid for LAD		$t_{LBKHOV3}$	–	2.3	ns	
Local bus clock to LALE assertion		$t_{LBKHOV4}$	–	2.3	ns	(3)

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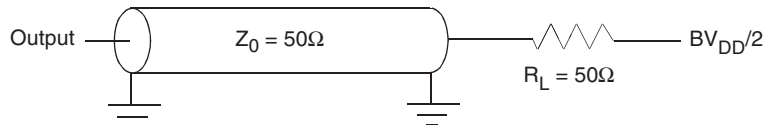
Table 11-2. Local Bus General Timing Parameters ($OV_{DD} = 3.3V$ DC) (Continued)

Parameter	Configuration	Symbol ⁽¹⁾	Min	Max	Unit	Notes
Output hold from local bus clock (except LAD/LDP and LALE)		$t_{LBKHOX1}$	0.7	–	ns	
Output hold from local bus clock for LAD/LDP		$t_{LBKHOX2}$	0.7	–	ns	
Local bus clock to output high Impedance (except LAD/LDP and LALE)		$t_{LBKHOZ1}$	–	2.5	ns	(5)
Local bus clock to output high impedance for LAD/LDP		$t_{LBKHOZ2}$	–	2.5	ns	(5)

- Notes:
- The symbols used for timing specifications herein follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
 - All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
 - All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
 - Input timings are measured at the pin.
 - For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
 - t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
 - Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
 - Guaranteed by design.

Figure 11-1 provides the AC test load for the local bus.

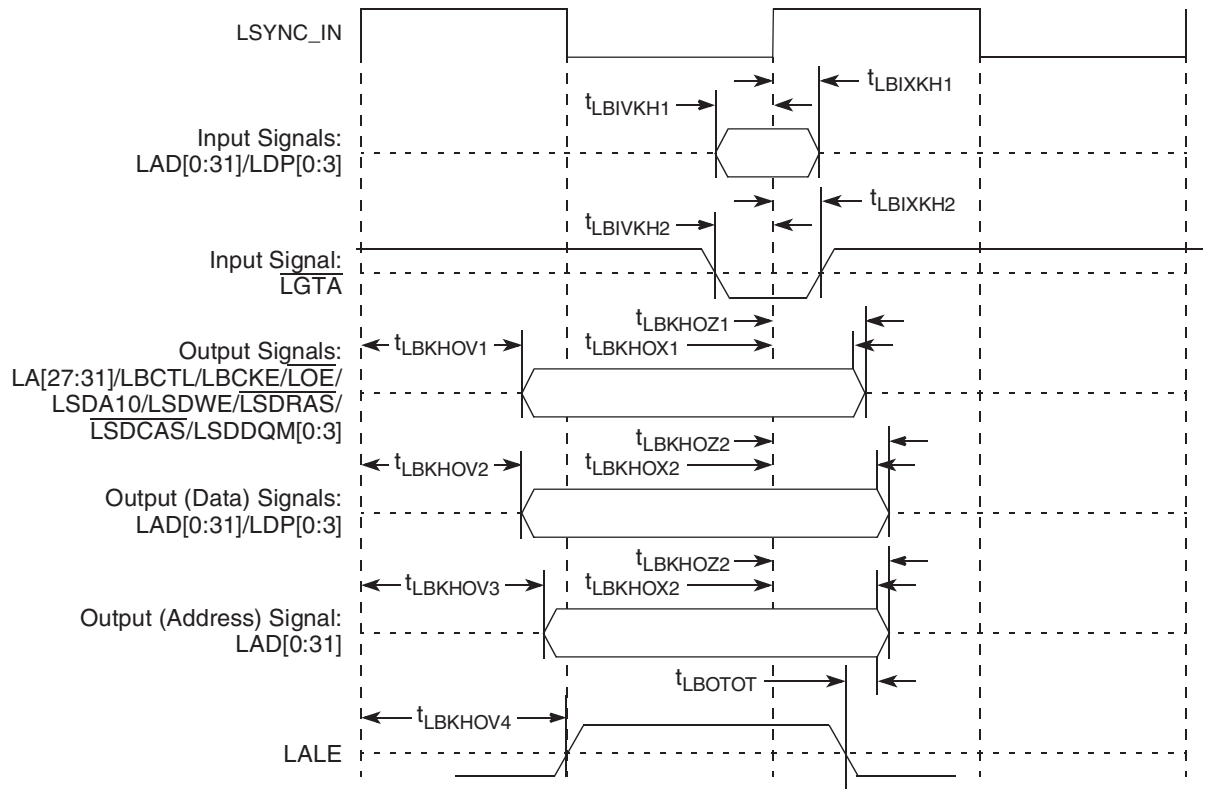
Figure 11-1. Local Bus AC Test Load



Note: PLL bypass mode is recommended when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 MHz, LBIU PLL is recommended to be enabled.

Figure 11-2 to Figure 11-4 on page 46 show the local bus signals.

Figure 11-2. Local Bus Signals, Non-Special Signals Only (PLL Enabled)



- Notes:
1. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. Only the falling edge of LALE matters with respect to the specification.
 2. In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of t_{LBKHK1} . In this mode, signals are latched at the rising edge of the internal clock and are captured at falling edge of the internal clock.

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Figure 11-3. Local Bus Signals (PLL Bypass Mode)

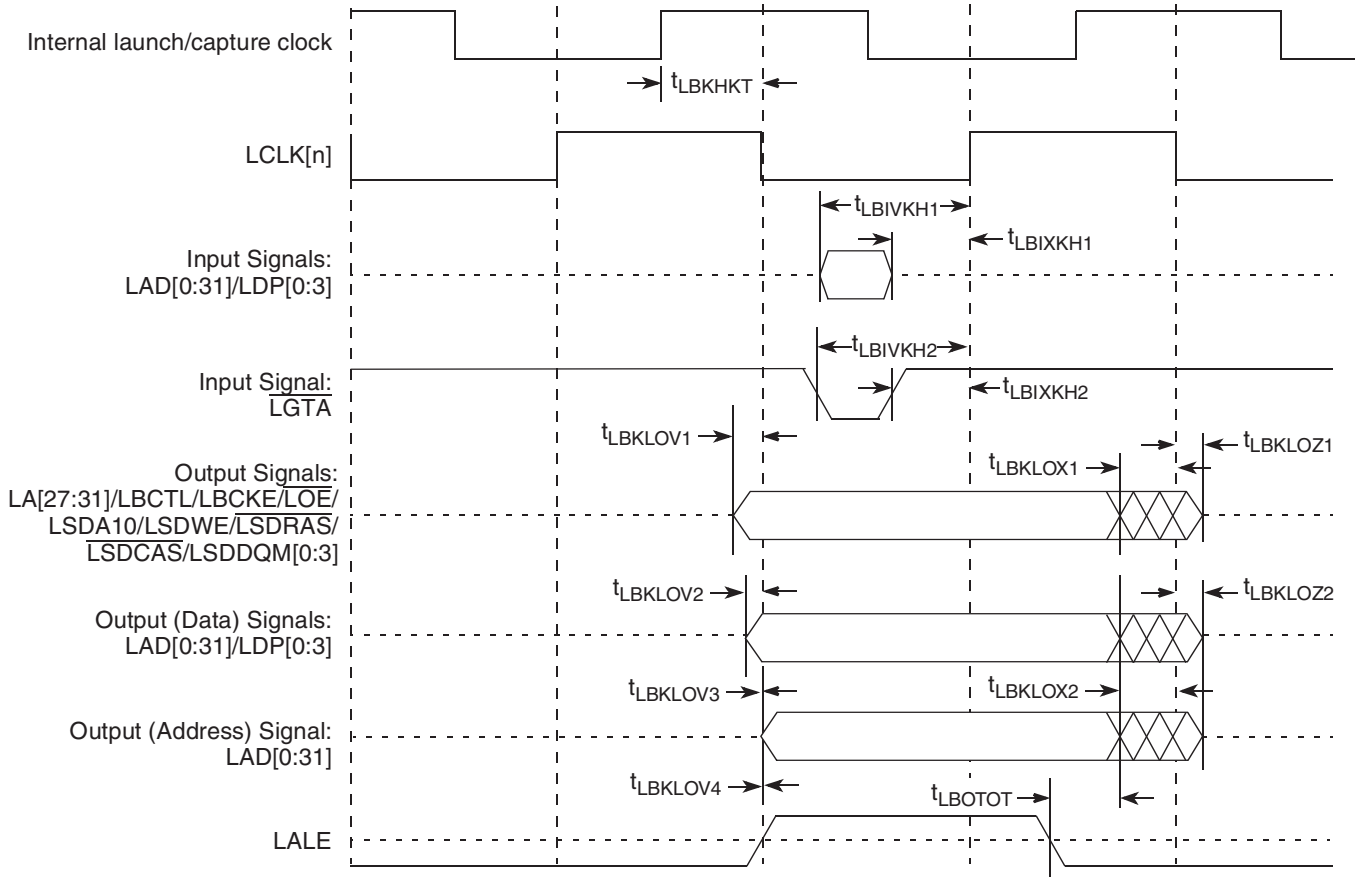


Table 11-3 describes the general timing parameters of the local bus interface at $V_{DD} = 3.3V$ DC with PLL disabled.

Table 11-3. Local Bus General Timing Parameters: PLL Bypassed

Parameter	Symbol ⁽¹⁾	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	–	ns	(2)
Local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	
Internal launch/capture clock to LCLK delay	t_{LBKHKT}	2.3	3.9	ns	(8)
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	5.7	–	ps	(4)(5)
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	5.6	–	ns	(4)(5)
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	-1.8	–	ns	(4)(5)
LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	-1.3	–	ns	(4)(5)
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	–	ns	(4)(5)
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKLOV1}$	–	-0.3	ns	(6)
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	–	-0.1	ns	
Local bus clock to address valid for LAD	$t_{LBKLOV3}$	–	0	ns	(4)
Local bus clock to LALE assertion	$t_{LBKLOV4}$	–	0	ns	(4)
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKLOX1}$	-3.2	–	ns	(4)
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	-3.2	–	ns	(4)
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKLOZ1}$	–	0.2	ns	(7)
Local bus clock to output high impedance for LAD/LDP	$t_{LBKLOZ2}$	–	0.2	ns	(7)

- Notes:
- The symbols used for timing specifications herein follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state}) (\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
 - All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by t_{LBKHKT} .
 - Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
 - All signals are measured from $BV_{DD}/2$ of the rising edge of local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3V signaling levels.
 - Input timings are measured at the pin.
 - The value of t_{LBOTOT} is the measurement of the minimum time between the negation of LALE and any change in LAD.
 - For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
 - Guaranteed by characterization.

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Figure 11-4. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (PLL Enabled)

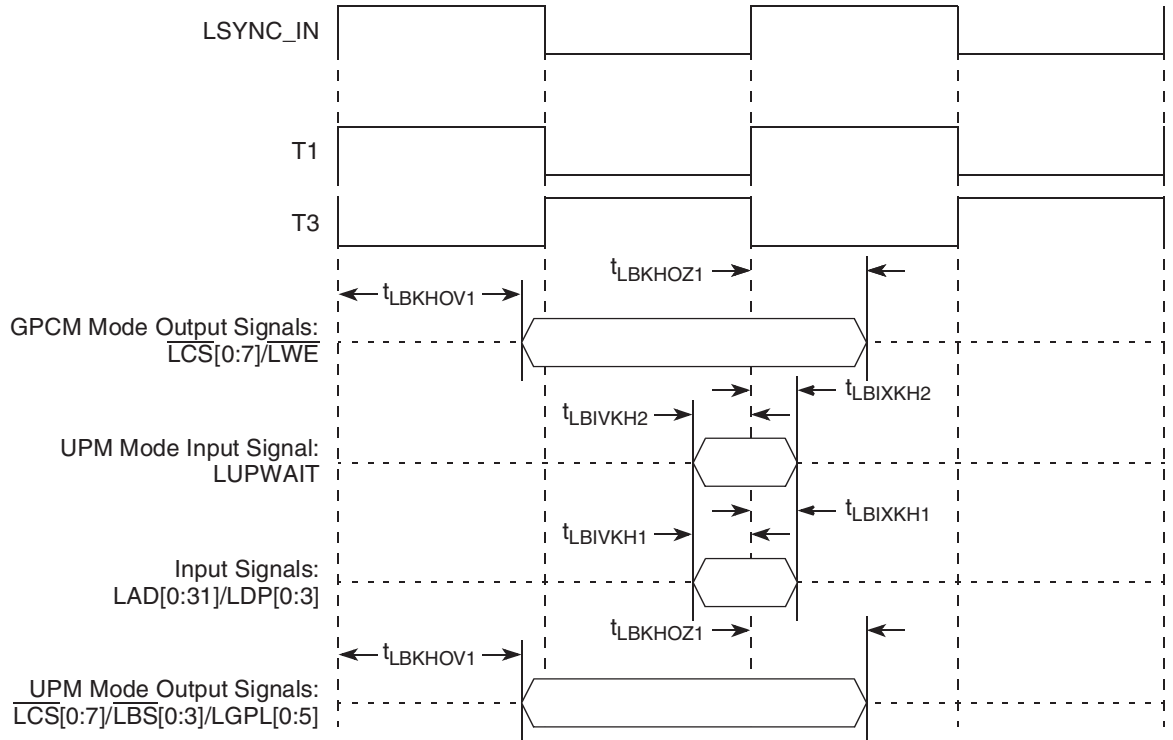
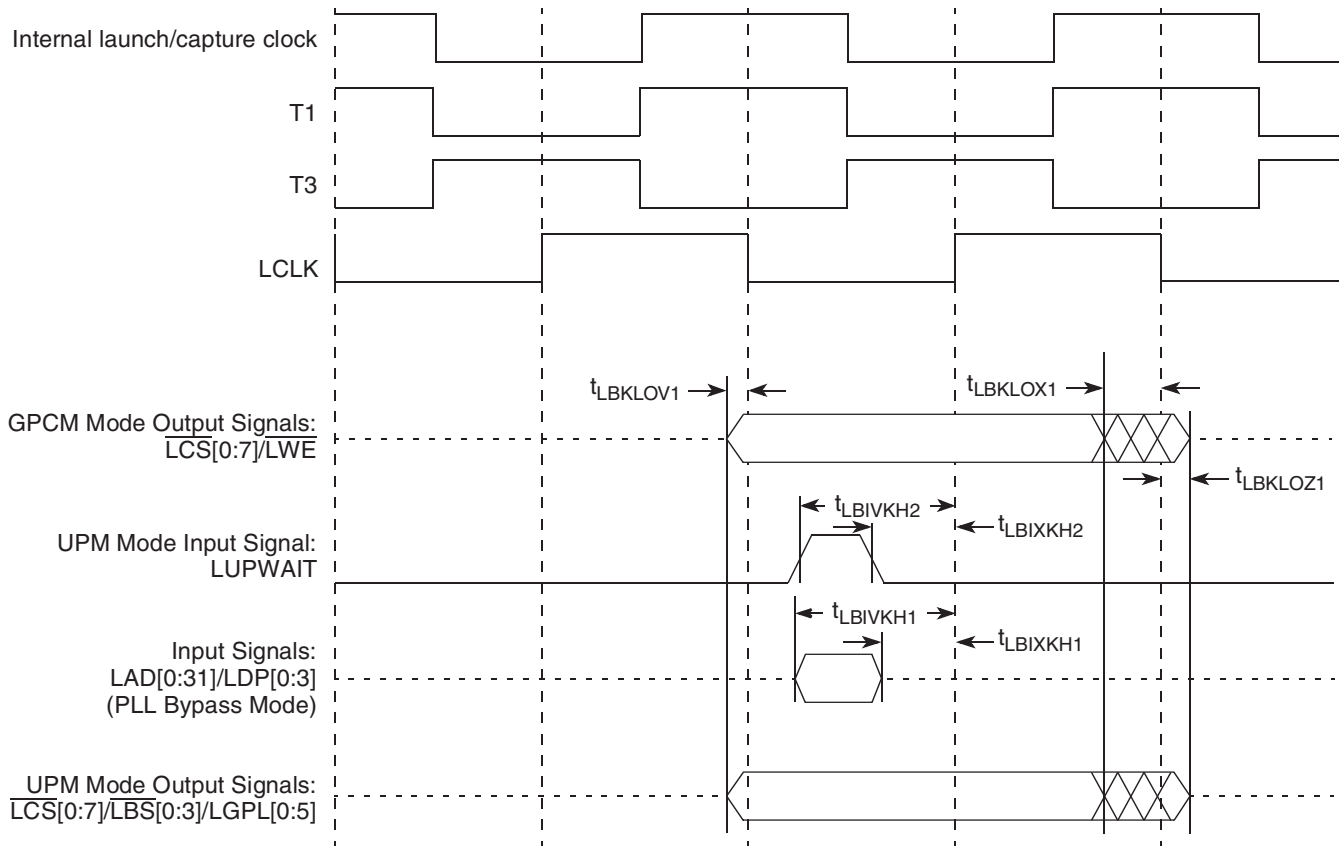


Figure 11-5. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (PLL Bypass Mode)



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Figure 11-6. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)

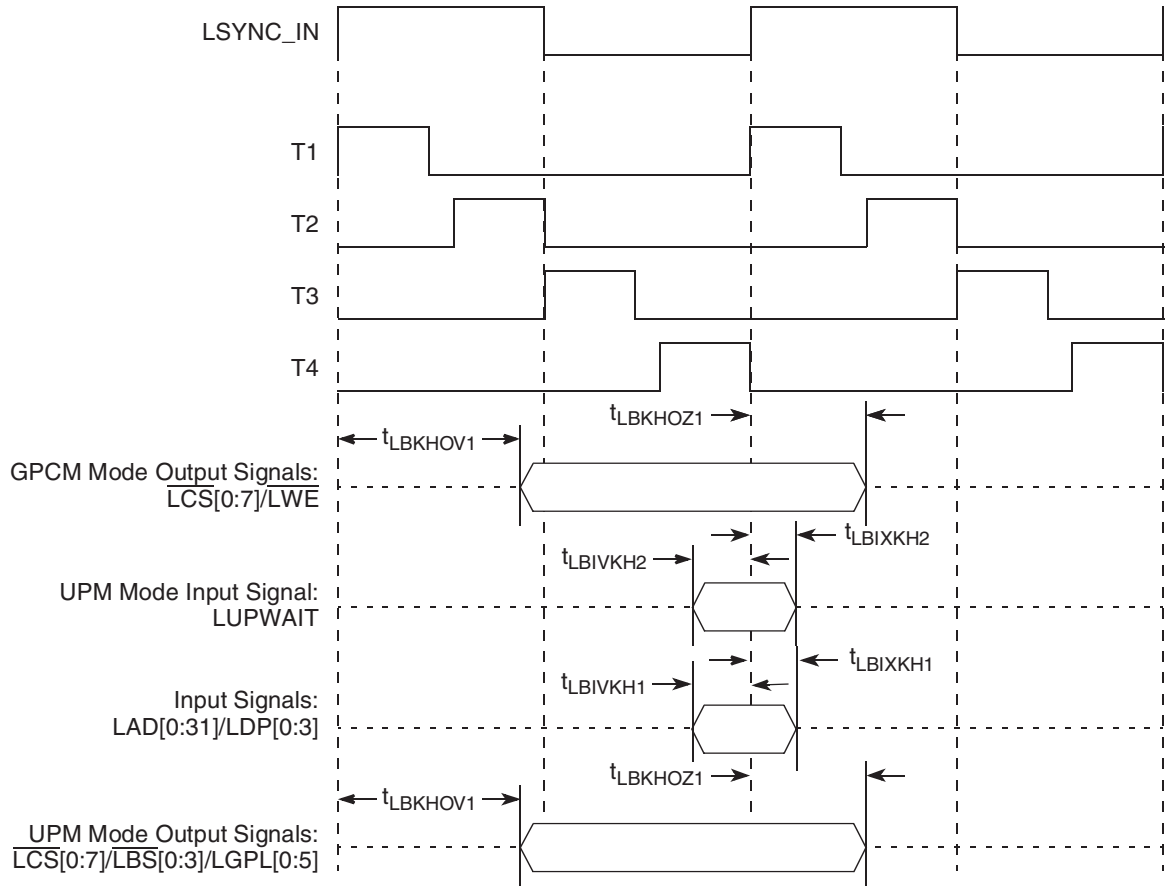
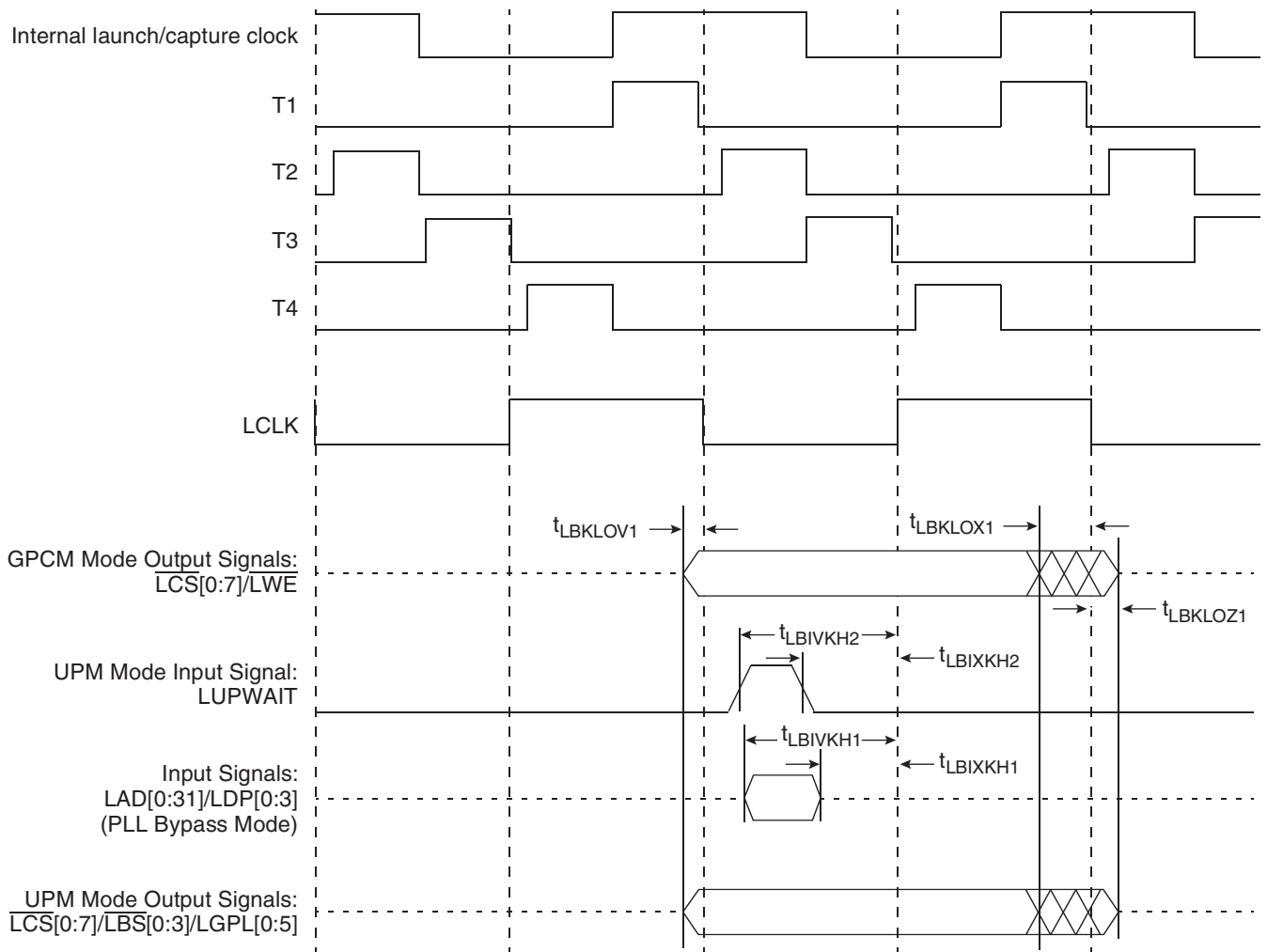


Figure 11-7. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)



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12. JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the PC8641.

12.1 JTAG DC Electrical Characteristics

Table 12-1 provides the DC electrical characteristics for the JTAG interface.

Table 12-1. JTAG DC Electrical Characteristics

Parameter	Symbol ⁽¹⁾	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3V$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current ($V_{IN}^{(1)} = 0V$ or $V_{IN} = V_{DD}$)	I_{IN}	–	±5	µA
High-level output voltage ($OV_{DD} = \text{min}$, $I_{OH} = -100 \mu A$)	V_{OH}	$OV_{DD} - 0.2$	–	V
Low-level output voltage ($OV_{DD} = \text{min}$, $I_{OL} = 100 \mu A$)	V_{OL}	–	0.2	V

Note: 1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 3-1 on page 6 and Table 3-2 on page 7.

Table 12-2 provides the JTAG AC timing specifications as defined in Figure 12-2 on page 51 through Figure 12-4 on page 52.

Table 12-2. JTAG AC Timing Specifications (Independent of SYSCLK)⁽¹⁾ (At Recommended Operating Conditions (see Table 3-2 on page 7))

Parameter	Symbol ⁽²⁾	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t_{JTG}	30	–	ns	
JTAG external clock pulse width measured at 1.4V	t_{JTKHKL}	15	–	ns	
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	(6)
\overline{TRST} assert time	t_{TRST}	25	–	ns	(3)
Input setup times: - Boundary-scan data - TMS, TDI	t_{JTDVKH} t_{JTIVKH}	15 0	– –	ns	(4)
Input hold times: - Boundary-scan data - TMS, TDI	t_{JTDXKH} t_{JTIXKH}	20 25	– –	ns	(4)

Table 12-2. JTAG AC Timing Specifications (Independent of SYSCLK)⁽¹⁾ (At Recommended Operating Conditions (see Table 3-2 on page 7) (Continued)

Parameter	Symbol ⁽²⁾	Min	Max	Unit	Notes
Valid times: - Boundary-scan data - TDO	t_{JTKLDV} t_{JTKLOV}	4 4	20 25	ns	(5)
Output hold times: - Boundary-scan data - TDO	t_{JTKLDX} t_{JTKLOX}	30 30	– –	ns	(5)
JTAG external clock to output high impedance: - Boundary-scan data - TDO	t_{JTKLDZ} t_{JTKLOZ}	3 3	19 9	ns	(5)(6)

- Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load (see Figure 12-1). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
 2. The symbols used for timing specifications herein follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
 3. \overline{TRST} is an asynchronous level sensitive signal. The setup time is for test purposes only.
 4. Non-JTAG signal input timing with respect to t_{TCLK} .
 5. Non-JTAG signal output timing with respect to t_{TCLK} .
 6. Guaranteed by design.

Figure 12-1 provides the AC test load for TDO and the boundary-scan outputs.

Figure 12-1. AC Test Load for the JTAG Interface

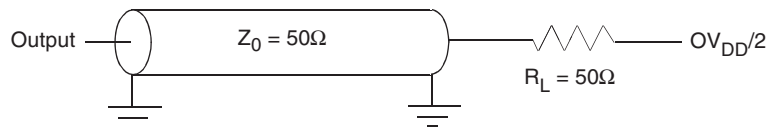
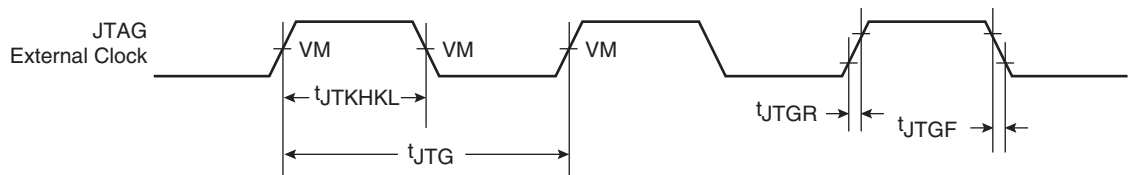


Figure 12-2 provides the JTAG clock input timing diagram.

Figure 12-2. JTAG Clock Input Timing Diagram



Note: VM = Midpoint Voltage ($OV_{DD}/2$).

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Figure 12-3 provides the $\overline{\text{TRST}}$ timing diagram.

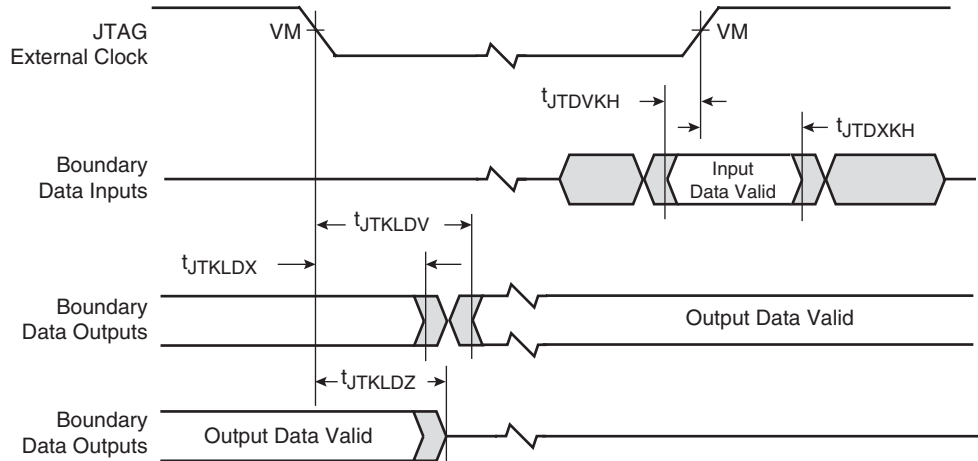
Figure 12-3. $\overline{\text{TRST}}$ Timing Diagram



Note: VM = Midpoint Voltage ($OV_{DD}/2$).

Figure 12-4 provides the boundary-scan timing diagram.

Figure 12-4. Boundary-scan Timing Diagram



Note: VM = Midpoint Voltage ($OV_{DD}/2$).

13. I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the PC8641.

13.1 I²C DC Electrical Characteristics

Table 13-1 provides the DC electrical characteristics for the I²C interfaces.

Table 13-1. I²C DC Electrical Characteristics (At Recommended Operating Conditions with OV_{DD} of $3.3V \pm 5\%$)

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	-0.3	$0.3 \times OV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	(1)
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	(2)
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$ (max))	I_I	-10	10	μA	(3)
Capacitance for each I/O pin	C_I	-	10	pF	

- Notes:
- Output voltage (open drain or open collector) condition = 3 mA sink current.
 - Refer to the PC8641 PowerQUICC III Integrated Host Processor Reference Manual for information on the digital filter used.
 - I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

13.2 I²C AC Electrical Specifications

Table 13-2 provides the AC timing parameters for the I²C interfaces.

Table 13-2. I²C AC Electrical Specifications (All Values Refer to V_{IH} (min) and V_{IL} (max) Levels (see Table 13-1 on page 52))

Parameter	Symbol ⁽¹⁾	Min	Max	Unit
SCL clock frequency	f _{I2C}	0	400	kHz
Low period of the SCL clock	t _{I2CL} ⁽⁴⁾	1.3	–	μs
High period of the SCL clock	t _{I2CH} ⁽⁴⁾	0.6	–	μs
Setup time for a repeated START condition	t _{I2SVKH} ⁽⁴⁾	0.6	–	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXKL} ⁽⁴⁾	0.6	–	μs
Data setup time	t _{I2DVKH} ⁽⁴⁾	100	–	ns
Data input hold time: - CBUS compatible masters - I ² C bus devices	t _{I2DXKL}	– 0 ⁽²⁾	– –	μs
Data output delay time	t _{I2OVKL}	–	0.9 ⁽³⁾	μs
Set-up time for STOP condition	t _{I2PVKH}	0.6	–	μs
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	–	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	0.1 × OV _{DD}	–	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	0.2 × OV _{DD}	–	V

- Notes:
- The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
 - As a transmitter, the PC8641 provides a delay time of at least 300 ns for the SDA signal (referred to the Vihmin of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When PC8641 acts as the I²C bus master while transmitting, PC8641 drives both SCL and SDA. As long as the load on SCL and SDA are balanced, PC8641 would not cause unintended generation of Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for PC8641 as transmitter, the following setting is recommended for the FDR bit field of the I2CFDR register to ensure both the desired I²C SCL clock frequency and SDA output delay time are achieved, assuming that the desired I²C SCL clock frequency is 400 KHz and the Digital Filter Sampling Rate Register (I2CDFSRR) is programmed with its default setting of 0x10 (decimal 16):

I ² C Source Clock Frequency	333 MHz	266 MHz	200 MHz	133 MHz
FDR Bit Setting	0x2A	0x05	0x26	0x00
Actual FDR Divider Selected	896	704	512	384
Actual I ² C SCL Frequency Generated	371 KHz	378 KHz	390 KHz	346 KHz

For the detail of I²C frequency calculation, refer to the application note AN2919 “Determining the I²C Frequency Divider Ratio for SCL”. Note that the I²C Source Clock Frequency is half of the MPX clock frequency for PC8641.

- The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- Guaranteed by design.

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Figure 13-1 provides the AC test load for the I²C.

Figure 13-1. I²C AC Test Load

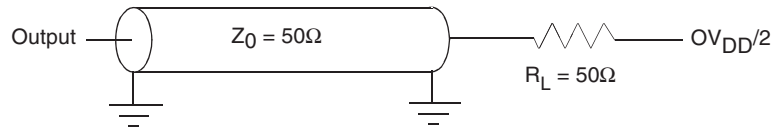
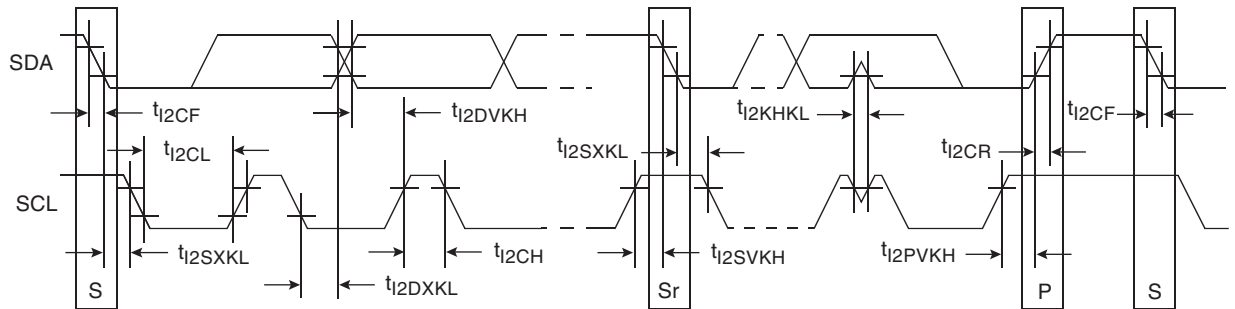


Figure 13-2 shows the AC timing diagram for the I²C bus.

Figure 13-2. I²C Bus AC Timing Diagram



14. High-Speed Interfaces

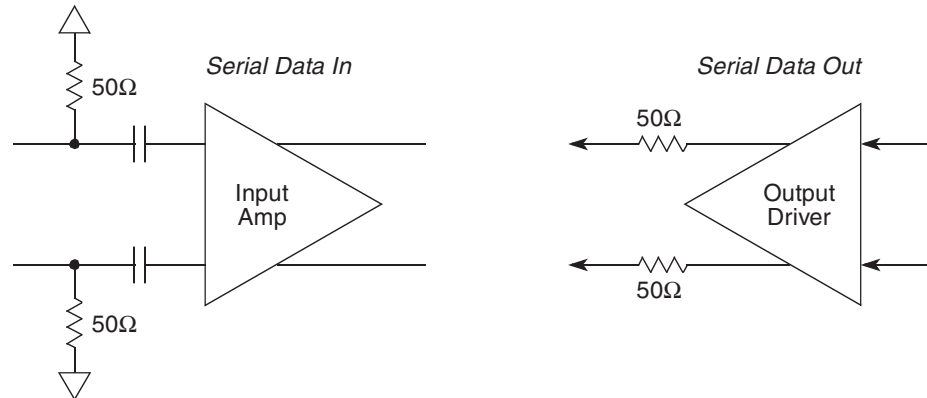
This section describes the common DC electrical specifications for the high-speed interconnect interfaces (Serial RapidIO and PCI Express) of the PC8641.

14.1 DC Requirements for SerDes Reference Clocks

The SerDes reference clocks are $\overline{SD1_REF_CLK}$, $\overline{SD1_REF_CLK}$, $\overline{SD2_REF_CLK}$ and $\overline{SD2_REF_CLK}$.

- Recommended minimum operating voltage is -0.4V; recommended maximum operating voltage is 1.32V; Maximum absolute voltage is 1.72V.
- Each differential clock input has an internal 50Ω termination to GND. The reference clock must be able to drive this termination. The input is AC-coupled on chip following the termination.
- The amplitude of the clock must be at least a 400-mV differential peak-peak for single-ended clock. If driven differentially, each signal wire needs to drive ±100 mV around common mode voltage.
- The differential reference clock ($\overline{SDn_REF_CLK}/\overline{SDn_REF_CLK}$) input is HCSL compatible DC coupled or LVDS compatible with AC coupling.

Figure 14-1. Driver and Receiver of SerDes (PCI Express, Serial RapidIO, and $\overline{SDn_REF_CLK}/\overline{SDn_REF_CLK}$)



15. PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the PC8641.

15.1 DC Requirements for PCI Express $\overline{SDn_REF_CLK}$ and $\overline{SDn_REF_CLK}$

For more information, see [Section 14.1 "DC Requirements for SerDes Reference Clocks"](#) on page 54.

15.2 AC Requirements for PCI Express SerDes Clocks

[Table 15-1](#) lists AC requirements.

Table 15-1. $\overline{SDn_REF_CLK}$ and $\overline{SDn_REF_CLK}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	–	10	–	ns	–
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	–	–	100	ps	–
t_{REFPJ}	Phase jitter. Deviation edge location in edge location with respect to mean	-50	–	50	ps	–

15.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ± 300 ppm tolerance.

15.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the Transport and Data Link layer please use the PCI EXPRESS Base Specification. REV. 1.0a document.

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15.4.1 Differential Transmitter (TX) Output

Table 15-2 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 15-2. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note (1).
$V_{TX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.8		1.2	V	$V_{TX-DIFFp-p} = 2 * V_{TX-D+} - V_{TX-D-} $ See Note (2).
$V_{TX-DE-RATIO}$	De- Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note (2).
T_{TX-EYE}	Minimum TX Eye Width	0.70			UI	The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes (2) and (3).
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.			0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0V$) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes (2) and (3).
$T_{TX-RISE, TTX-FALL}$	D+/D- TX Output Rise/Fall Time	0.125			UI	See Notes (2) and (4)
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage			20	mV	$V_{TX-CM-ACp} = \text{RMS}(V_{TXD+} - V_{TXD-} /2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = DC_{(avg)}$ of $ V_{TX-D+} - V_{TX-D-} /2$ See Note (2)
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage During LO and Electrical Idle	0		100	mV	$ V_{TX-CM-DC}(\text{during LO}) - V_{TX-CM-Idle-DC}(\text{During Electrical Idle}) \leq 100$ mV $V_{TX-CM-DC} = DC_{(avg)}$ of $ V_{TX-D+} - V_{TX-D-} /2$ [LO] $V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $ V_{TX-D+} - V_{TX-D-} /2$ [Electrical Idle] See Note (2).
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode between D+ and D-	0		25	mV	$ V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-} \leq 25$ mV $V_{TX-CM-DC-D+} = DC_{(avg)}$ of $ V_{TX-D+} $ $V_{TX-CM-DC-D-} = DC_{(avg)}$ of $ V_{TX-D-} $ See Note (2).
$V_{TX-IDLE-DIFFp}$	Electrical Idle differential Peak Output Voltage	0		20	mV	$V_{TX-IDLE-DIFFp} = V_{TX-IDLE-D+} - V_{TX-IDLE-D-} \leq 20$ mV See Note (2).
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection			600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present. See Note (5).
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0		3.6	V	The allowed DC Common Mode voltage under any conditions. See Note (5).
$I_{TX-SHORT}$	TX Short Circuit Current Limit			90	mA	The total current the Transmitter can provide when shorted to its ground.
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50			UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set.

Table 15-2. Differential Transmitter (TX) Output Specifications (Continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical idle after sending an Electrical Idle ordered set			20	UI	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from LO.
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an Electrical idle condition			20	UI	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle.
$RL_{TX-DIFF}$	Differential Return Loss	12			dB	Measured over 50 MHz to 1.25 GHz. See Note ⁽⁴⁾
RL_{TX-CM}	Common Mode Return Loss	6			dB	Measured over 50 MHz to 1.25 GHz. See Note ⁽³⁾
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential mode Low Impedance.
Z_{TX-DC}	Transmitter DC Impedance	40			Ω	Required TX D+ as wellall states.
$L_{TX-SKEW}$	Lane-to-Lane Output Skew			500 + 2 UI	ps	Static skew between any two Transmitter Lanes within a single Link.
C_{TX}	AC Coupling Capacitor	75		200	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note ⁽⁸⁾
$T_{crosslink}$	Crosslink Random Timeout	0		1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port. See Note ⁽⁷⁾ .

- Notes:
1. No test load is necessarily associated with this value.
 2. Specified at the measurement point into a timing and voltage compliance test load as shown in [Figure 15-3 on page 61](#) and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in [Figure 15-1 on page 58](#).)
 3. A $T_{TX-EYE} = 0.70$ UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX} = 0.30$ UI for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
 4. The Transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 Ω probes; see [Figure 15-3 on page 61](#)). Note that the series capacitors C_{TX} is optional for the return loss measurement.
 5. Measured between 20-80% at transmitter package pins into a test load as shown in [Figure 15-3](#) for both V_{TX-D+} and V_{TX-D-} .
 6. See Section 4.3.1.8 of the PCI Express Base Specifications Rev 1.0a.
 7. See Section 4.2.6.3 of the PCI Express Base Specifications Rev 1.0a.
 8. PC8641D SerDes transmitter does not have C_{TX} built-in. An external AC Coupling capacitor is required.

15.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in [Figure 15-1](#) is specified using the passive compliance/test measurement load (see [Figure 15-3 on page 61](#)) in place of any real PCI Express interconnect + RX component.

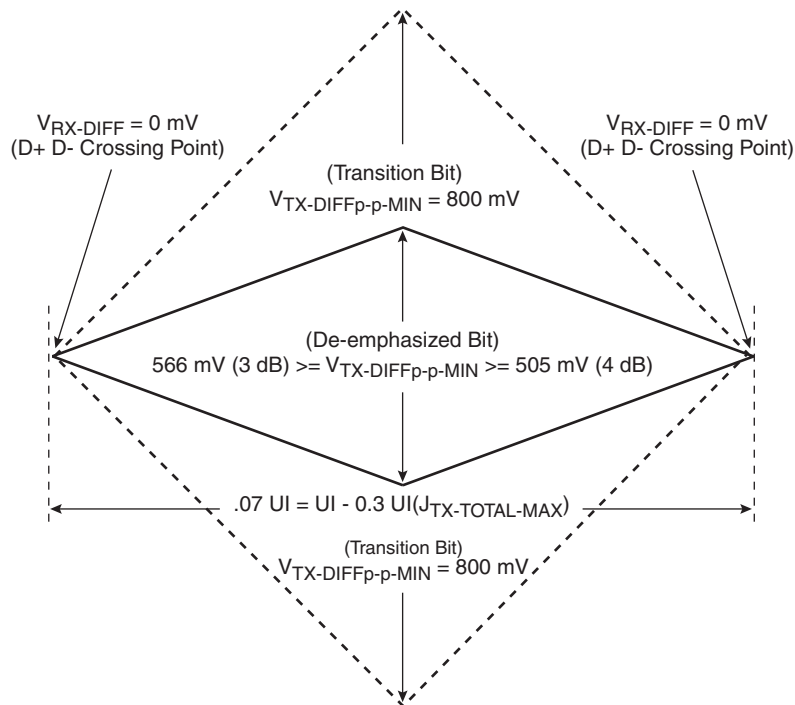
There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

Note: It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (i.e., least squares and median deviation fits).

Figure 15-1. Minimum Transmitter Timing and Voltage Output Compliance Specifications



15.4.3 Differential Receiver (RX) Input Specifications

Table 15-3 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 15-3. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note (1).
$V_{RX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.175		1.200	V	$V_{RX-DIFFp-p} = 2 * V_{RX-D+} - V_{RX-D-} $ See Note (2).
T_{RX-EYE}	Minimum Receiver Eye Width	0.4			UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes (2) and (3).
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0V$) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes (2)(3)(7).
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage			150	mV	$V_{RX-CM-ACp} = V_{RXD+} - V_{RXD-} /2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)} \text{ of } V_{RX-D+} - V_{RX-D-} /2$ See Note (2)
$RL_{RX-DIFF}$	Differential Return Loss	15			dB	Measured over 50 MHz to 1.25 GHz with the D+ and D-lines biased at +300 mV and -300 mV, respectively. See Note (4)
RL_{RX-CM}	Common Mode Return Loss	6			dB	Measured over 50 MHz to 1.25 GHz with the D+ and D-lines biased at 0V. See Note (4)
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω	RX DC Differential (5)
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω	Required RX D+ as well as D-DC Impedance (50 ± 20% tolerance). See Notes (2) and (5)
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200 k			Ω	Required RX D+ as well as D-DC Impedance when the Receiver terminations do not have power. See Note (6)
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65		175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 * V_{RX-D+} - V_{RX-D-} $ Measured at the package pins of the Receiver
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time			10	ms	An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.
$L_{TX-SKEW}$	Total Skew			20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (e.g. COM and one to five Symbols) at the RX as well as any delay differences arising from the interconnect itself.

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- Notes:
1. No test load is necessarily associated with this value.
 2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in [Figure 15-3 on page 61](#) should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in [Figure 15-2 on page 61](#)). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
 3. A $T_{RX-EYE} = 0.40$ UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
 4. The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50Ω probes - see [Figure 15-3](#)). Note: that the series capacitors CTX is optional for the return loss measurement.
 5. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
 6. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
 7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

15.5 Receiver Compliance Eye Diagrams

The RX eye diagram in [Figure 15-2](#) is specified using the passive compliance/test measurement load (see [Figure 15-3](#)) in place of any real PCI Express RX component.

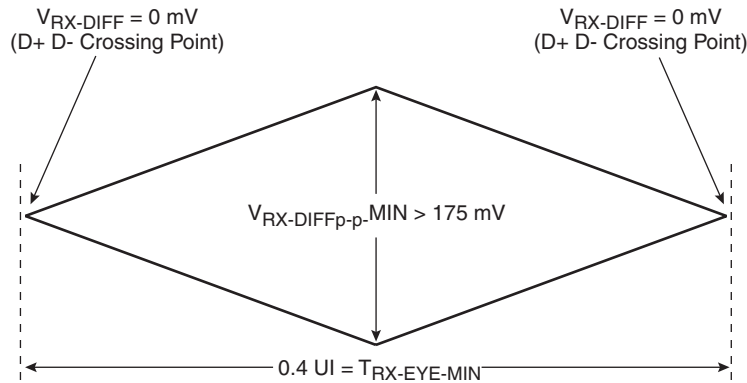
Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see [Figure 15-3](#)) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in [Figure 15-2](#)) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

Note: The reference impedance for return loss measurements is 50Ω to ground for both the D+ and D- line (i.e., as measured by a Vector Network Analyzer with 50Ω probes; see [Figure 15-3](#)). Note that the series capacitors, CTX, are optional for the return loss measurement.

Figure 15-2. Minimum Receiver Eye Timing and Voltage Compliance Specification

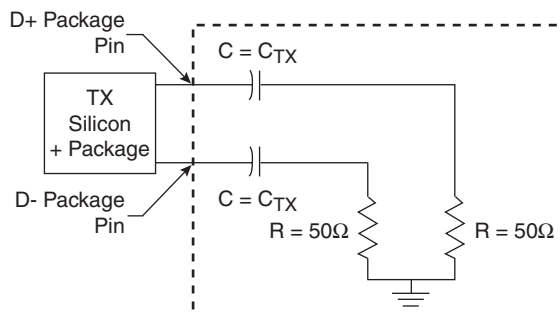


15.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 15-3.

Note: The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

Figure 15-3. Compliance Test/Measurement Load



16. Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the PC8641, for the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links.

Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that will accept signals from both the short run and long run transmitter specifications.

The short run transmitter should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

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The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of ± 100 ppm. The worst case frequency difference between any transmit and receive clock will be 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

16.1 DC Requirements for Serial RapidIO SDn_REF_CLK and $\overline{SDn_REF_CLK}$

For more information, see [Section 14.1 "DC Requirements for SerDes Reference Clocks"](#) on page 54.

16.2 AC Requirements for Serial RapidIO SDn_REF_CLK and $\overline{SDn_REF_CLK}$

[Table 16-1](#) lists AC requirements.

Table 16-1. SDn_REF_CLK and $\overline{SDn_REF_CLK}$ AC Requirements

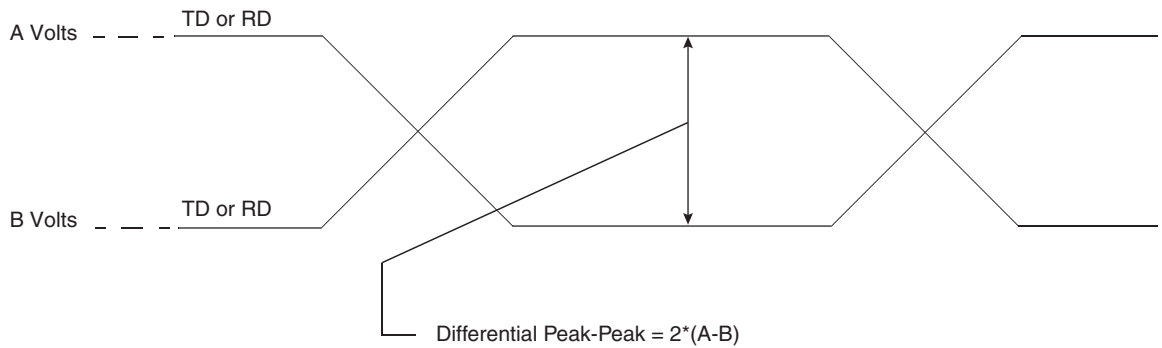
Symbol	Parameter Description	Min	Typical	Max	Units	Comments
t_{REF}	REFCLK cycle time	-	10(8)	-	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	-	-	80	ps	-
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	-40	-	40	ps	-

16.3 Signal Definitions

LP-Serial links use differential signaling. This section defines terms used in the description and specification of differential signals. [Figure 16-1 on page 63](#) shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and \overline{TD}) or a receiver input (RD and \overline{RD}). Each signal swings between A Volts and B Volts where $A > B$. Using these waveforms, the definitions are as follows:

1. The transmitter output signals and the receiver input signals TD, \overline{TD} , RD and \overline{RD} each have a peak-to-peak swing of $A - B$ Volts.
2. The differential output signal of the transmitter, V_{OD} , is defined as $V_{TD} - V_{\overline{TD}}$
3. The differential input signal of the receiver, V_{ID} , is defined as $V_{RD} - V_{\overline{RD}}$
4. The differential output signal of the transmitter and the differential input signal of the receiver each range from $A - B$ to $-(A - B)$ Volts.
5. The peak value of the differential transmitter output signal and the differential receiver input signal is $A - B$ Volts.
6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is $2 * (A - B)$ Volts.

Figure 16-1. Differential Peak-Peak Voltage of Transmitter or Receiver



To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25V and each of its outputs, \overline{TD} and TD, has a swing that goes between 2.5V and 2.0V. Using these values, the peak-to-peak voltage swing of the signals TD and \overline{TD} is 500 mV p-p. The differential output signal ranges between 500 mV and -500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

16.4 Equalization

With the use of high speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification.

To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

16.5 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in [Section 9.1 on page 26](#). The goal of this standard is that electrical designs for serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

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16.6 Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than

- -10 dB for (Baud Frequency)/10 < Freq(f) < 625 MHz, and
- -10 dB + 10log(f/625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100 Ohm resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%-80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB and 15 ps at 3.125 GB.

Table 16-2. Short Run Transmitter AC Timing Specifications: 1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V _O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V _{DIFFPP}	500	1000	mV p-p	
Deterministic Jitter	J _D		0.17	UI p-p	
Total Jitter	J _T		0.35	UI p-p	
Multiple output skew	S _{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	± 100 ppm

Table 16-3. Short Run Transmitter AC Timing Specifications: 2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V _O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V _{DIFFPP}	500	1000	mV p-p	
Deterministic Jitter	J _D		0.17	UI p-p	
Total Jitter	J _T		0.35	UI p-p	
Multiple output skew	S _{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	± 100 ppm

Table 16-4. Short Run Transmitter AC Timing Specifications: 3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	
Deterministic Jitter	J_D		0.17	UI p-p	
Total Jitter	J_T		0.35	UI p-p	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	± 100 ppm

Table 16-5. Long Run Transmitter AC Timing Specifications: 1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	
Deterministic Jitter	J_D		0.17	UI p-p	
Total Jitter	J_T		0.35	UI p-p	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	± 100 ppm

Table 16-6. Long Run Transmitter AC Timing Specifications: 2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	
Deterministic Jitter	J_D		0.17	UI p-p	
Total Jitter	J_T		0.35	UI p-p	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	± 100 ppm

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Table 16-7. Long Run Transmitter AC Timing Specifications: 3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	
Deterministic Jitter	J_D		0.17	UI p-p	
Total Jitter	J_T		0.35	UI p-p	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	± 100 ppm

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the Transmitter Output Compliance Mask shown in Figure 16-2 with the parameters specified in Table 16-8 on page 67 when measured at the output pins of the device and the device is driving a 100 Ohm $\pm 5\%$ differential resistive load. The output eye pattern of an LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the Transmitter Output Compliance Mask when pre-emphasis is disabled or minimized.

Figure 16-2. Transmitter Output Compliance Mask

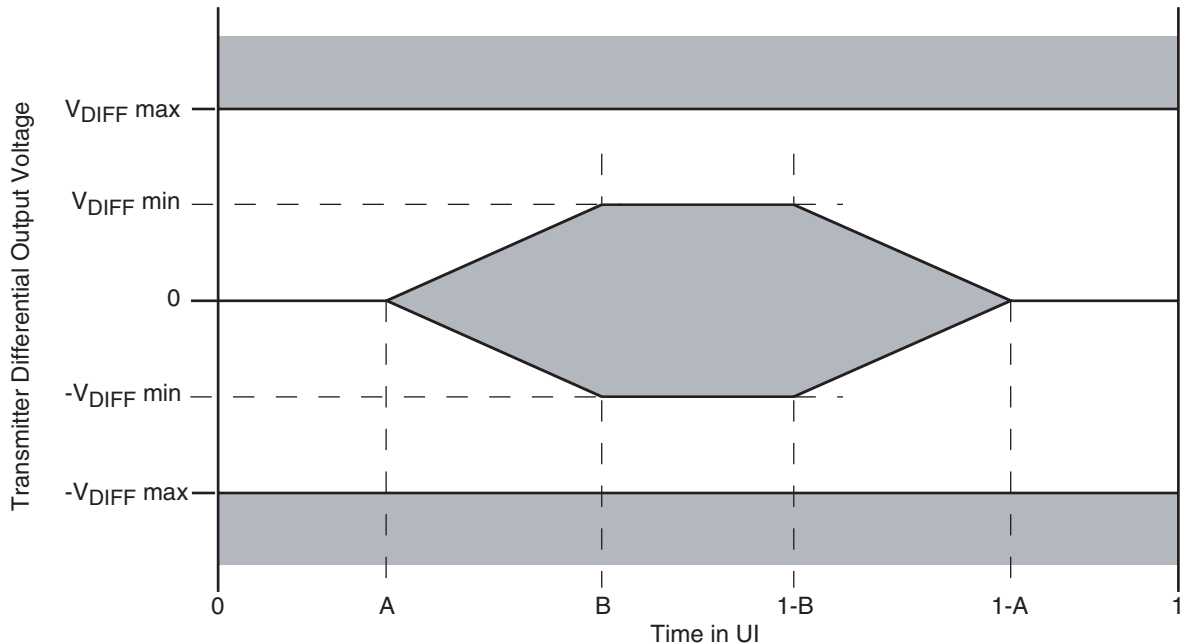


Table 16-8. Transmitter Differential Output Eye Diagram Parameters

Transmitter Type	V _{DIFFmin} (mV)	V _{DIFFmax} (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

16.7 Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance shall result in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8)*(Baud Frequency). This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100Ω resistive for differential return loss and 25Ω resistive for common mode.

Table 16-9. Receiver AC Timing Specifications – 1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V _{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J _D	0.37		UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J _{DR}	0.55		UI p-p	Measured at receiver
Total Jitter Tolerance ⁽¹⁾	J _T	0.65		UI p-p	Measured at receiver
Multiple Input Skew	S _{MI}		24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10 ⁻¹²		
Unit Interval	UI	800	800	ps	± 100 ppm

Note: 1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 16-3 on page 69](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

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Table 16-10. Receiver AC Timing Specifications: 2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI p-p	Measured at receiver
Total Jitter Tolerance ⁽¹⁾	J_T	0.65		UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}		24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	400	400	ps	± 100 ppm

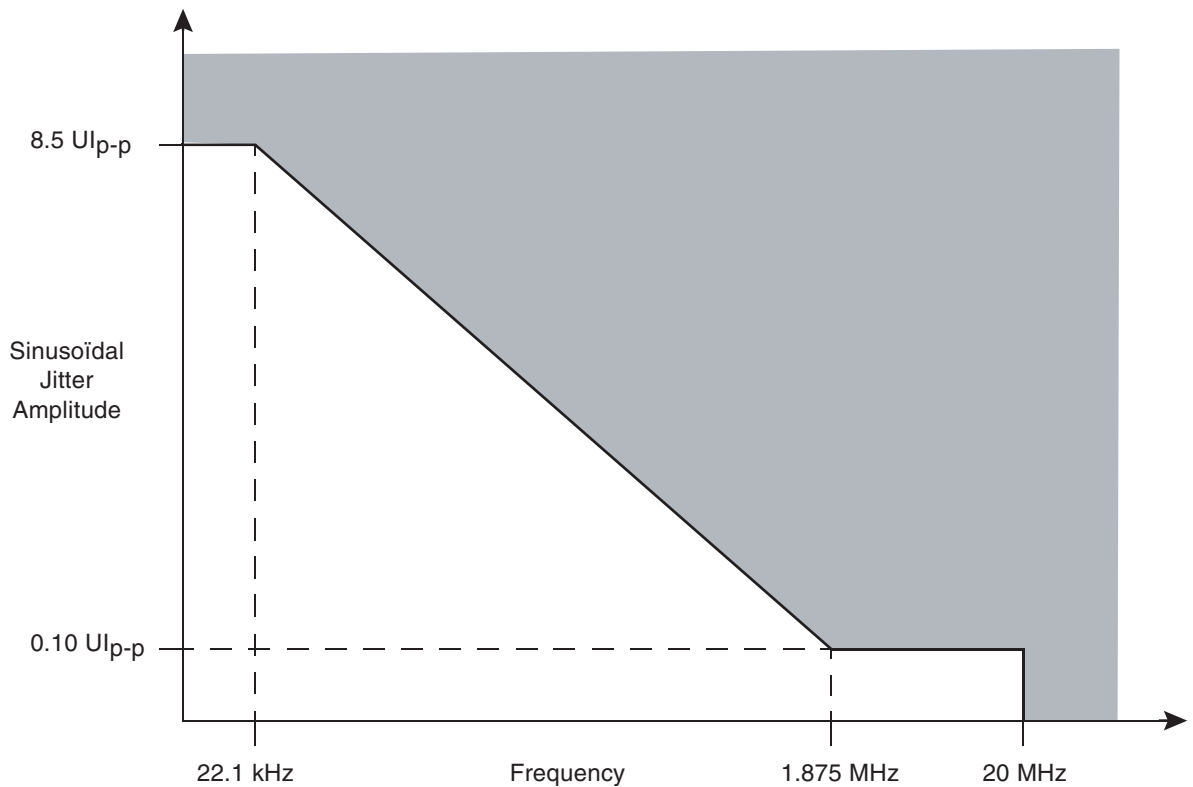
Note: Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 16-3 on page 69](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 16-11. Receiver AC Timing Specifications: 3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI p-p	Measured at receiver
Total Jitter Tolerance ⁽¹⁾	J_T	0.65		UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}		22	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	320	320	ps	± 100 ppm

Note: 1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 16-3](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects

Figure 16-3. Single Frequency Sinusoidal Jitter Limits



16.8 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding Bit Error Rate specification ([Table 16-9 on page 67](#), [Table 16-10 on page 68](#), [Table 16-11 on page 68](#)) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the Receiver Input Compliance Mask shown in [Figure 16-4 on page 70](#) with the parameters specified in [Table 16-12 on page 70](#). The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a $100\Omega \pm 5\%$ differential resistive load.

Figure 16-4. Receiver Input Compliance Mask

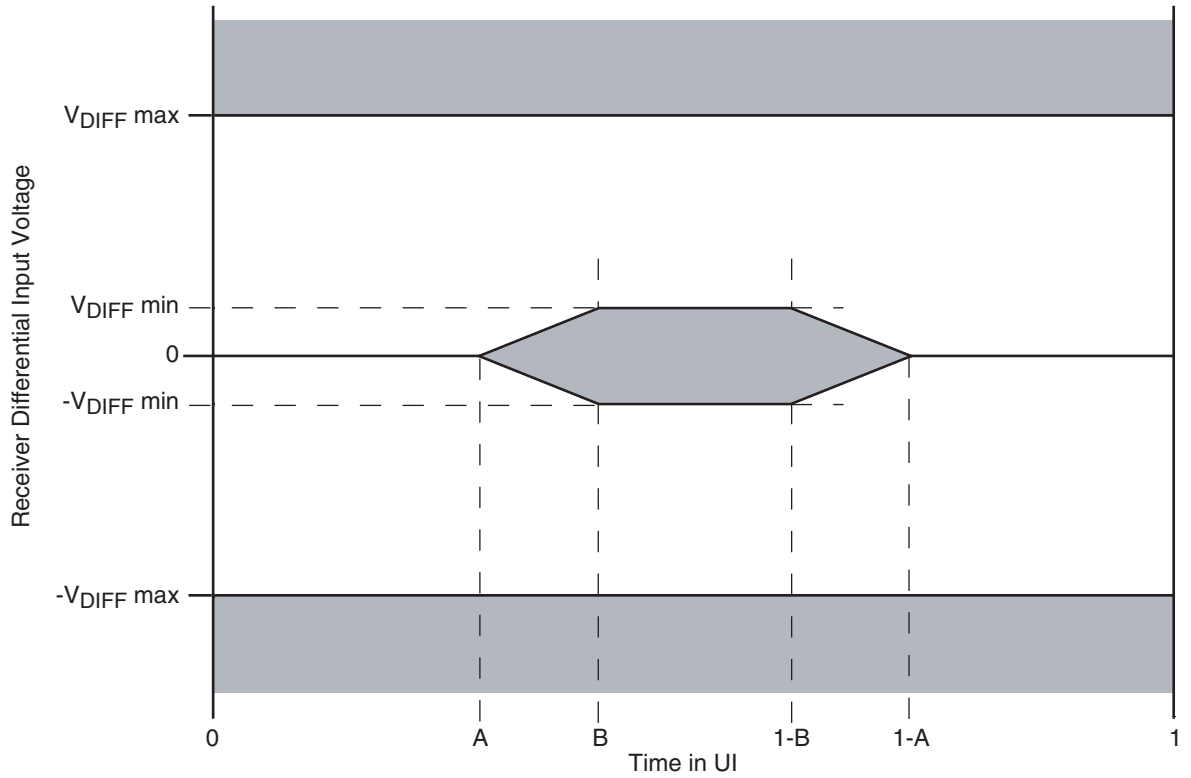


Table 16-12. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type	V _{DIFF} min (mV)	V _{DIFF} max (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

16.9 Measurement and Test Requirements

Since the LP-Serial electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002, the measurement and test requirements defined here are similarly guided by Clause 47. In addition, the CJPAT test pattern defined in Annex 48A of IEEE802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

16.9.1 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for template measurements is the Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of IEEE802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12} .

The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100 Ohms resistive $\pm 5\%$ differential to 2.5 GHz.

16.9.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of IEEE802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 Volts differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE802.3ae.

16.9.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ohms resistive $\pm 5\%$ differential to 2.5 GHz.

16.9.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 8.6 and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 8.6 is then added to the signal and the test load is replaced by the receiver being tested.

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17. Package

This section details package parameters and dimensions.

17.1 Package Parameters for the PC8641

The package parameters are as provided in the following list. The package type is 33 mm x 33 mm, 1023 pins. There are two package options: high-lead Flip Chip-Ceramic Ball Grid Array (FC-CBGA), and lead-free (FC-CBGA).

For all package types:

Die size	12.4 mm x 15.3 mm
Package outline	33 mm x 33 mm
Interconnects	1023
Pitch	1 mm
Total Capacitor count	43 caps; 100 nF each

For high-lead FC-CBGA (package option: HCTE⁽¹⁾ GH)

Maximum module height	2.97 mm
Minimum module height	2.47 mm
Solder Balls	89.5% Pb 10.5% Sn
Ball diameter (typical ⁽²⁾)	0.60 mm

For RoHS lead-free FC-CBGA (package option: HiTCE SH)

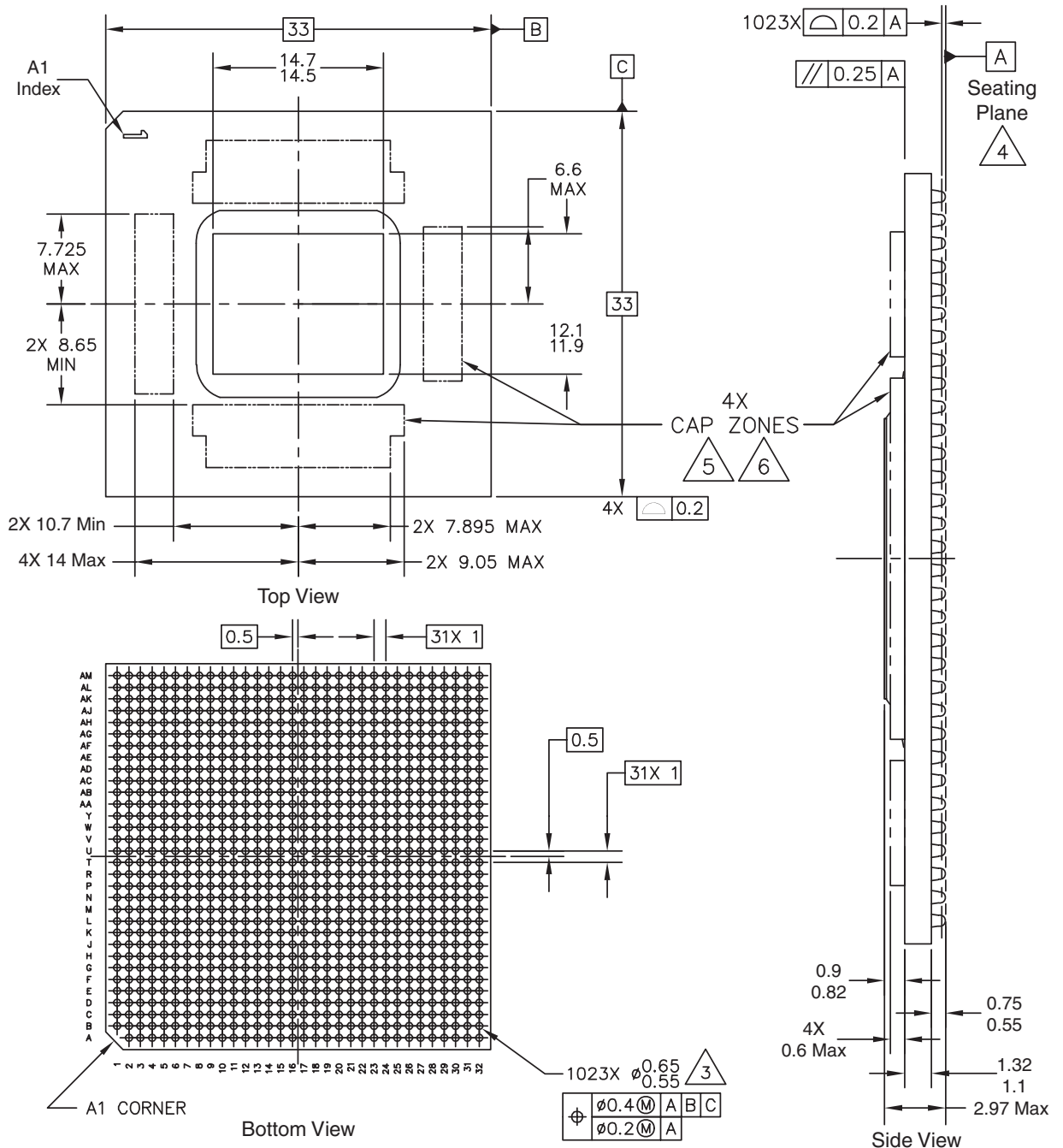
Maximum module height	2.72 mm
Minimum module height	2.27 mm
Solder Balls	95.5% Sn 4.0% Ag 0.5% Cu
Ball diameter (typical ⁽²⁾)	0.60 mm

- Notes:
1. High-coefficient of thermal expansion.
 2. Typical ball diameter is before reflow.

17.2 Mechanical Dimensions of the PC8641 FC-CBGA

The mechanical dimensions and bottom surface nomenclature of the PC8641D (dual core) and PC8641 (single core) high-lead FC-CBGA (package option: HCTE HX) and lead-free FC-CBGA (package option: HCTE SH) are shown respectively in [Table 17-1](#) and [Table 17-2](#) on page 74.

Figure 17-1. PC8641 High-head FC-CBGA Dimensions



- Notes:
1. All dimensions are in millimeters.
 2. Dimensions and tolerances per ASME Y14.5M-1994.
 3. Maximum solder ball diameter measured parallel to datum A.

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- Notes:
1. All dimensions are in millimeters.
 2. Dimensions and tolerances per ASME Y14.5M-1994.
 3. Maximum solder ball diameter measured parallel to datum A.
 4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
 5. Capacitors may not be present on all devices.
 6. Caution must be taken not to short capacitors or expose metal capacitor pads on package top.
 7. All dimensions symmetrical about centerlines unless otherwise specified.
 8. Note that for PC8641 (single core) the solder balls for the following signals/pins are not populated in the package: VDD_Core1 (R16, R18, R20, T17, T19, T21, T23, U16, U18, U22, V17, V19, V21, V23, W16, W18, W20, W22, Y17, Y19, Y21, Y23, AA16, AA18, AA20, AA22, AB23, AC24) and SENSEVDD_Core1 (U20).

18. Signal Listings

Table 18-1 provides the pin assignments for the signals. Notes for the signal changes on the single core device (PC8641) are italicized and prefixed by “S”.

Table 18-1. PC8641 Signal Reference by Functional Block

Name ⁽¹⁾	Package Pin Number	Pin Type	Power Supply	Notes
DDR Memory Interface 1 Signals⁽²⁾⁽³⁾				
D1_MDQ[0:63]	D15, A14, B12, D12, A15, B15, B13, C13, C11, D11, D9, A8, A12, A11, A9, B9, F11, G12, K11, K12, E10, E9, J11, J10, G8, H10, L9, L7, F10, G9, K9, K8, AC6, AC7, AG8, AH9, AB6, AB8, AE9, AF9, AL8, AM8, AM10, AK11, AH8, AK8, AJ10, AK10, AL12, AJ12, AL14, AM14, AL11, AM11, AM13, AK14, AM15, AJ16, AK18, AL18, AJ15, AL15, AL17, AM17	I/O	D1_GV _{DD}	
D1_MECC[0:7]	M8, M7, R8, T10, L11, L10, P9, R10	I/O	D1_GV _{DD}	
D1_MDM[0:8]	C14, A10, G11, H9, AD7, AJ9, AM12, AK16, N10	O	D1_GV _{DD}	
D1_MDQS[0:8]	A13, C10, H12, J7, AE8, AM9, AK13, AK17, N9	I/O	D1_GV _{DD}	
$\overline{D1_MDQS}$ [0:8]	D14, B10, H13, J8, AD8, AL9, AJ13, AM16, P10	I/O	D1_GV _{DD}	
D1_MBA[0:2]	AA8, AA10, T9	O	D1_GV _{DD}	
D1_MA[0:15]	Y10, W8, W9, V7, V8, U6, V10, U9, U7, U10, Y9, T6, T8, AE12, R7, P6	O	D1_GV _{DD}	
$\overline{D1_MWE}$	AB11	O	D1_GV _{DD}	
$\overline{D1_MRAS}$	AB12	O	D1_GV _{DD}	
$\overline{D1_MCAS}$	AC10	O	D1_GV _{DD}	
$\overline{D1_MCS}$ [0:3]	AB9, AD10, AC12, AD11	O	D1_GV _{DD}	
D1_MCKE[0:3]	P7, M10, N8, M11	O	D1_GV _{DD}	(23)
D1_MCK[0:5]	W6, E13, AH11, Y7, F14, AG10	O	D1_GV _{DD}	
$\overline{D1_MCK}$ [0:5]	Y6, E12, AH12, AA7, F13, AG11	O	D1_GV _{DD}	
D1_MODT[0:3]	AC9, AF12, AE11, AF10	O	D1_GV _{DD}	
D1_MDIC[0:1]	E15, G14	IO	D1_GV _{DD}	(27)
D1_MV _{REF}	AM18	DDR Port 1 reference voltage	D1_GV _{DD} /2	(3)
DDR Memory Interface 2 Signals⁽²⁾⁽³⁾				

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Table 18-1. PC8641 Signal Reference by Functional Block (Continued)

Name ⁽¹⁾	Package Pin Number	Pin Type	Power Supply	Notes
D2_MDQ[0:63]	A7, B7, C5, D5, C8, D8, D6, A5, C4, A3, D3, D2, A4, B4, C2, C1, E3, E1, H4, G1, D1, E4, G3, G2, J4, J2, L1, L3, H3, H1, K1, L4, AA4, AA2, AD1, AD2, Y1, AA1, AC1, AC3, AD5, AE1, AG1, AG2, AC4, AD4, AF3, AF4, AH3, AJ1, AM1, AM3, AH1, AH2, AL2, AL3, AK5, AL5, AK7, AM7, AK4, AM4, AM6, AJ7	I/O	D2_GV _{DD}	
D2_MECC[0:7]	H6, J5, M5, M4, G6, H7, M2, M1	I/O	D2_GV _{DD}	
D2_MDM[0:8]	C7, B3, F4, J1, AB1, AE2, AK1, AM5, K6	O	D2_GV _{DD}	
D2_MDQS[0:8]	B6, B1, F1, K2, AB3, AF1, AL1, AL6, L6	I/O	D2_GV _{DD}	
$\overline{D2_MDQS}$ [0:8]	A6, A2, F2, K3, AB2, AE3, AK2, AJ6, K5	I/O	D2_GV _{DD}	
D2_MBA[0:2]	W5, V5, P3	O	D2_GV _{DD}	
D2_MA[0:15]	W1, U4, U3, T1, T2, T3, T5, R2, R1, R5, V4, R4, P1, AH5, P4, N1	O	D2_GV _{DD}	
$\overline{D2_MWE}$	Y4	O	D2_GV _{DD}	
$\overline{D2_MRAS}$	W3	O	D2_GV _{DD}	
$\overline{D2_MCAS}$	AB5	O	D2_GV _{DD}	
$\overline{D2_MCS}$ [0:3]	Y3, AF6, AA5, AF7	O	D2_GV _{DD}	
D2_MCKE[0:3]	N6, N5, N2, N3	O	D2_GV _{DD}	(23)
D2_MCK[0:5]	U1, F5, AJ3, V2, E7, AG4	O	D2_GV _{DD}	
$\overline{D2_MCK}$ [0:5]	V1, G5, AJ4, W2, E6, AG5	O	D2_GV _{DD}	
D2_MODT[0:3]	AE6, AG7, AE5, AH6	O	D2_GV _{DD}	
D2_MDIC[0:1]	F8, F7	IO	D2_GV _{DD}	(27)
D2_MV _{REF}	A18	DDR Port 2 reference voltage	D2_GV _{DD} /2	(3)
High Speed I/O Interface 1 (SERDES 1)⁽⁴⁾				
SD1_TX[0:7]	L26, M24, N26, P24, R26, T24, U26, V24	O	SV _{DD}	
$\overline{SD1_TX}$ [0:7]	L27, M25, N27, P25, R27, T25, U27, V25	O	SV _{DD}	
SD1_RX[0:7]	J32, K30, L32, M30, T30, U32, V30, W32	I	SV _{DD}	
$\overline{SD1_RX}$ [0:7]	J31, K29, L31, M29, T29, U31, V29, W31	I	SV _{DD}	
SD1_REF_CLK	N32	I	SV _{DD}	
$\overline{SD1_REF_CLK}$	N31	I	SV _{DD}	
SD1_IMP_CAL_TX	Y26	Analog	SV _{DD}	(19)
SD1_IMP_CAL_RX	J28	Analog	SV _{DD}	(30)
SD1_PLL_TPD	U28	O	SV _{DD}	(13)(17)
SD1_PLL_TPA	T28	Analog	SV _{DD}	(13)(18)
SD1_DLL_TPD	N28	O	SV _{DD}	(13)(17)
SD1_DLL_TPA	P31	Analog	SV _{DD}	(13)(18)
High Speed I/O Interface 2 (SERDES 2)⁽⁴⁾				
SD2_TX[0:3]	Y24, AA27, AB25, AC27	O	SV _{DD}	
SD2_TX[4:7]	AE27, AG27, AJ27, AL27	O	SV _{DD}	(34)
$\overline{SD2_TX}$ [0:3]	Y25, AA28, AB26, AC28	O	SV _{DD}	

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Table 18-1. PC8641 Signal Reference by Functional Block (Continued)

Name ⁽¹⁾	Package Pin Number	Pin Type	Power Supply	Notes
SD2_TX[4:7]	AE28, AG28, AJ28, AL28	O	SV _{DD}	(34)
SD2_RX[0:3]	Y30, AA32, AB30, AC32	I	SV _{DD}	(32)
SD2_RX[4:7]	AH30, AJ32, AK30, AL32	I	SV _{DD}	(32)(35)
SD2_RX[0:3]	Y29, AA31, AB29, AC31	I	SV _{DD}	
SD2_RX[4:7]	AH29, AJ31, AK29, AL31	I	SV _{DD}	(35)
SD2_REF_CLK	AE32	I	SV _{DD}	
SD2_REF_CLK	AE31	I	SV _{DD}	
SD2_IMP_CAL_TX	AM29	Analog	SV _{DD}	(19)
SD2_IMP_CAL_RX	AA26	Analog	SV _{DD}	(30)
SD2_PLL_TPD	AF29	O	SV _{DD}	(13)(17)
SD2_PLL_TPA	AF31	Analog	SV _{DD}	(13)(18)
SD2_DLL_TPD	AD29	O	SV _{DD}	(13)(17)
SD2_DLL_TPA	AD30	Analog	SV _{DD}	(13)(18)
Special Connection Requirement pins				
No Connects	K24, K25, P28, P29, W26, W27, AD25, AD26	–	–	(13)
Reserved	H30, R32, V28, AG32	–	–	(14)
Reserved	H29, R31, W28, AG31	–	–	(15)
Reserved	AD24, AG26	–	–	(16)
Ethernet Miscellaneous Signals⁽⁵⁾				
EC1_GTX_CLK125	AL23	I	LV _{DD}	(39)
EC2_GTX_CLK125	AM23	I	TV _{DD}	(39)
EC_MDC	G31	O	OV _{DD}	
EC_MDIO	G32	I/O	OV _{DD}	
eTSEC Port 1 Signals⁽⁵⁾				
TSEC1_TXD[0:7]/ GPOUT[0:7]	AF25, AC23, AG24, AG23, AE24, AE23, AE22, AD22	O	LV _{DD}	(6)(10)
TSEC1_TX_EN	AB22	O	LV _{DD}	(36)
TSEC1_TX_ER	AH26	O	LV _{DD}	
TSEC1_TX_CLK	AC22	I	LV _{DD}	(40)
TSEC1_GTX_CLK	AH25	O	LV _{DD}	
TSEC1_CRS	AM24	I/O	LV _{DD}	(37)
TSEC1_COL	AM25	I	LV _{DD}	
TSEC1_RXD[0:7]/ GPIN[0:7]	AL25, AL24, AK26, AK25, AM26, AF26, AH24, AG25	I	LV _{DD}	(10)
TSEC1_RX_DV	AJ24	I	LV _{DD}	
TSEC1_RX_ER	AJ25	I	LV _{DD}	
TSEC1_RX_CLK	AK24	I	LV _{DD}	(40)
eTSEC Port 2 Signals⁽⁵⁾				

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Table 18-1. PC8641 Signal Reference by Functional Block (Continued)

Name ⁽¹⁾	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_TXD[0:3]/ GPOUT[8:15]	AB20, AJ23, AJ22, AD19	O	LV _{DD}	(6)(10)
TSEC2_TXD[4]/ GPOUT[12]	AH23	O	LV _{DD}	(6)(10)(38)
TSEC2_TXD[5:7]/ GPOUT[13:15]	AH21, AG22, AG21	O	LV _{DD}	(6)(10)
TSEC2_TX_EN	AB21	O	LV _{DD}	(36)
TSEC2_TX_ER	AB19	O	LV _{DD}	(6)(38)
TSEC2_TX_CLK	AC21	I	LV _{DD}	(40)
TSEC2_GTX_CLK	AD20	O	LV _{DD}	
TSEC2_CRS	AE20	I/O	LV _{DD}	(37)
TSEC2_COL	AE21	I	LV _{DD}	
TSEC2_RXD[0:7]/ GPIN[8:15]	AL22, AK22, AM21, AH20, AG20, AF20, AF23, AF22	I	LV _{DD}	(10)
TSEC2_RX_DV	AC19	I	LV _{DD}	
TSEC2_RX_ER	AD21	I	LV _{DD}	
TSEC2_RX_CLK	AM22	I	LV _{DD}	(40)
eTSEC Port 3 Signals⁽⁵⁾				
TSEC3_TXD[0:3]	AL21, AJ21, AM20, AJ20	O	TV _{DD}	(6)
TSEC3_TXD[4]/	AM19	O	TV _{DD}	
TSEC3_TXD[5:7]	AK21, AL20, AL19	O	TV _{DD}	(6)
TSEC3_TX_EN	AH19	O	TV _{DD}	(36)
TSEC3_TX_ER	AH17	O	TV _{DD}	
TSEC3_TX_CLK	AH18	I	TV _{DD}	(40)
TSEC3_GTX_CLK	AG19	O	TV _{DD}	
TSEC3_CRS	AE15	I/O	TV _{DD}	(37)
TSEC3_COL	AF15	I	TV _{DD}	
TSEC3_RXD[0:7]	AJ17, AE16, AH16, AH14, AJ19, AH15, AG16, AE19	I	TV _{DD}	
TSEC3_RX_DV	AG15	I	TV _{DD}	
TSEC3_RX_ER	AF16	I	TV _{DD}	
TSEC3_RX_CLK	AJ18	I	TV _{DD}	(40)
eTSEC Port 4 Signals⁽⁵⁾				
TSEC4_TXD[0:3]	AC18, AC16, AD18, AD17	O	TV _{DD}	(6)
TSEC4_TXD[4]	AD16	O	TV _{DD}	(25)
TSEC4_TXD[5:7]	AB18, AB17, AB16	O	TV _{DD}	(6)
TSEC4_TX_EN	AF17	O	TV _{DD}	(36)
TSEC4_TX_ER	AF19	O	TV _{DD}	
TSEC4_TX_CLK	AF18	I	TV _{DD}	(40)
TSEC4_GTX_CLK	AG17	O	TV _{DD}	(41)

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Table 18-1. PC8641 Signal Reference by Functional Block (Continued)

Name ⁽¹⁾	Package Pin Number	Pin Type	Power Supply	Notes
TSEC4_CRS	AB14	I/O	TV _{DD}	(37)
TSEC4_COL	AC13	I	TV _{DD}	
TSEC4_RXD[0:7]	AG14, AD13, AF13, AD14, AE14, AB15, AC14, AE17	I	TV _{DD}	
TSEC4_RX_DV	AC15	I	TV _{DD}	
TSEC4_RX_ER	AF14	I	TV _{DD}	
TSEC4_RX_CLK	AG13	I	TV _{DD}	(40)
Local Bus Signals⁽⁵⁾				
LAD[0:31]	A30, E29, C29, D28, D29, H25, B29, A29, C28, L22, M22, A28, C27, H26, G26, B27, B26, A27, E27, G25, D26, E26, G24, F27, A26, A25, C25, H23, K22, D25, F25, H22	I/O	OV _{DD}	(6)
LDP[0:3]	A24, E24, C24, B24	I/O	OV _{DD}	(6)(22)
LA[27:31]	J21, K21, G22, F24, G21	O	OV _{DD}	(6)(22)
$\overline{\text{LCS}}[0:4]$	A22, C22, D23, E22, A23	O	OV _{DD}	(7)
$\overline{\text{LCS}}[5]/\text{DMA_DREQ}[2]$	B23	O	OV _{DD}	(7)(9)(10)
$\overline{\text{LCS}}[6]/\text{DMA_DACK}[2]$	E23	O	OV _{DD}	(7)(10)
$\overline{\text{LCS}}[7]/\text{DMA_DDONE}[2]$	F23	O	OV _{DD}	(7)(10)
$\overline{\text{LWE}}[0:3]/$ LSDDQM[0:3]/ $\overline{\text{LBS}}[0:3]$	E21, F21, D22, E20	O	OV _{DD}	(6)
LBCTL	D21	O	OV _{DD}	
LALE	E19	O	OV _{DD}	
LGPL0/LSDA10	F20	O	OV _{DD}	(25)
LGPL1/LSDWE	H20	O	OV _{DD}	(25)
LGPL2/ $\overline{\text{LOE}}/$ $\overline{\text{LSDRAS}}$	J20	O	OV _{DD}	
LGPL3/ $\overline{\text{LSDCAS}}$	K20	O	OV _{DD}	(6)
LGPL4/ $\overline{\text{LGTA}}/$ LUPWAIT/LPBSE	L21	I/O	OV _{DD}	(42)
LGPL5	J19	O	OV _{DD}	(6)
LCKE	H19	O	OV _{DD}	
LCLK[0:2]	G19, L19, M20	O	OV _{DD}	
LSYNC_IN	M19	I	OV _{DD}	
LSYNC_OUT	D20	O	OV _{DD}	
DMA Signals⁽⁵⁾				
$\overline{\text{DMA_DREQ}}[0:1]$	E31, E32	I	OV _{DD}	
$\overline{\text{DMA_DREQ}}[2]/\overline{\text{LCS}}[5]$	B23	I	OV _{DD}	(9)(10)
$\overline{\text{DMA_DREQ}}[3]/\text{IRQ}[9]$	B30	I	OV _{DD}	(10)
$\overline{\text{DMA_DACK}}[0:1]$	D32, F30	O	OV _{DD}	
$\overline{\text{DMA_DACK}}[2]/\overline{\text{LCS}}[6]$	E23	O	OV _{DD}	(10)
$\overline{\text{DMA_DACK}}[3]/\text{IRQ}[10]$	C30	O	OV _{DD}	(9)(10)

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Table 18-1. PC8641 Signal Reference by Functional Block (Continued)

Name ⁽¹⁾	Package Pin Number	Pin Type	Power Supply	Notes
DMA_DDONE[0:1]	F31, F32	O	OV _{DD}	
DMA_DDONE[2]/LCS[7]	F23	O	OV _{DD}	(10)
DMA_DDONE[3]/IRQ[11]	D30	O	OV _{DD}	(9)(10)
Programmable Interrupt Controller Signals⁽⁵⁾				
MCP_0	F17	I	OV _{DD}	
MCP_1	H17	I	OV _{DD}	(12) S4
IRQ[0:8]	G28, G29, H27, J23, M23, J27, F28, J24, L23	I	OV _{DD}	
IRQ[9]/DMA_DREQ[3]	B30	I	OV _{DD}	(10)
IRQ[10]/DMA_DACK[3]	C30	I	OV _{DD}	(9)(10)
IRQ[11]/DMA_DDONE[3]	D30	I	OV _{DD}	(9)(10)
IRQ_OUT	J26	O	OV _{DD}	(7)(11)
DUART Signals⁽⁵⁾				
UART_SIN[0:1]	B32, C32	I	OV _{DD}	
UART_SOUT[0:1]	D31, A32	O	OV _{DD}	
UART_CTS[0:1]	A31, B31	I	OV _{DD}	
UART_RTS[0:1]	C31, E30	O	OV _{DD}	
I²C Signals				
IIC1_SDA	A16	I/O	OV _{DD}	(7)(11)
IIC1_SCL	B17	I/O	OV _{DD}	(7)(11)
IIC2_SDA	A21	I/O	OV _{DD}	(7)(11)
IIC2_SCL	B21	I/O	OV _{DD}	(7)(11)
System Control Signals⁽⁵⁾				
HRESET	B18	I	OV _{DD}	
HRESET_REQ	K18	O	OV _{DD}	
SMI_0	L15	I	OV _{DD}	
SMI_1	L16	I	OV _{DD}	(12) S4
SRESET_0	C20	I	OV _{DD}	
SRESET_1	C21	I	OV _{DD}	(12) S4
CKSTP_IN	L18	I	OV _{DD}	
CKSTP_OUT	L17	O	OV _{DD}	(7)(11)
READY/TRIG_OUT	J13	O	OV _{DD}	(10)(25)
Debug Signals⁽⁵⁾				
TRIG_IN	J14	I	OV _{DD}	
TRIG_OUT/READY	J13	O	OV _{DD}	(10)(25)
D1_MSRCID[0:1]/ LB_SRCID[0:1]	F15, K15	O	OV _{DD}	(6)(10)
D1_MSRCID[2]/ LB_SRCID[2]	K14	O	OV _{DD}	(10)(25)

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Table 18-1. PC8641 Signal Reference by Functional Block (Continued)

Name ⁽¹⁾	Package Pin Number	Pin Type	Power Supply	Notes
D1_MSRCID[3:4]/ LB_SRCID[3:4]	H15, G15	O	OV _{DD}	(10)
D2_MSRCID[0:4]	E16, C17, F16, H16, K16	O	OV _{DD}	
D1_MDVAL/LB_DVAL	J16	O	OV _{DD}	(10)
D2_MDVAL	D19	O	OV _{DD}	
Power Management Signals⁽⁵⁾				
ASLEEP	C19	O	OV _{DD}	
System Clocking Signals⁽⁵⁾				
SYSCLK	G16	I	OV _{DD}	
RTC	K17	I	OV _{DD}	(32)
CLK_OUT	B16	O	OV _{DD}	(23)
Test Signals⁽⁵⁾				
LSSD_MODE	C18	I	OV _{DD}	(26)
TEST_MODE[0:3]	C16, E17, D18, D16	I	OV _{DD}	(26)
JTAG Signals⁽⁵⁾				
TCK	H18	I	OV _{DD}	
TDI	J18	I	OV _{DD}	(24)
TDO	G18	O	OV _{DD}	(23)
TMS	F18	I	OV _{DD}	(24)
TRST	A17	I	OV _{DD}	(24)
Miscellaneous				
Spare	J17	–	–	(13)
GPOUT[0:7]/ TSEC1_TXD[0:7]	AF25, AC23, AG24, AG23, AE24, AE23, AE22, AD22	O	OV _{DD}	(6)(10)
GPIN[0:7]/ TSEC1_RXD[0:7]	AL25, AL24, AK26, AK25, AM26, AF26, AH24, AG25	I	OV _{DD}	(10)
GPOUT[8:15]/ TSEC2_TXD[0:7]	AB20, AJ23, AJ22, AD19, AH23, AH21, AG22, AG21	O	OV _{DD}	(10)
GPIN[8:15]/ TSEC2_RXD[0:7]	AL22, AK22, AM21, AH20, AG20, AF20, AF23, AF22	I	OV _{DD}	(10)
Additional Analog Signals				
TEMP_ANODE	AA11	Thermal	–	
TEMP_CATHODE	Y11	Thermal	–	
Sense, Power and GND Signals				
SENSEV _{DD} -Core0	M14	V _{DD} -Core0 sensing pin		(31)
SENSEV _{DD} -Core1	U20	V _{DD} -Core1 sensing pin		(12)(31) S1
SENSEV _{SS} -Core0	P14	Core0 GND sensing pin		(31)

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Table 18-1. PC8641 Signal Reference by Functional Block (Continued)

Name ⁽¹⁾	Package Pin Number	Pin Type	Power Supply	Notes
SENSEV _{SS-Core1}	V20	Core1 GND sensing pin		(12)(31) S3
SENSEV _{DD-PLAT}	N18	V _{DD-PLAT} sensing pin		(28)
SENSEV _{SS-PLAT}	P18	Platform GND sensing pin		(29)
D1_GV _{DD}	B11, B14, D10, D13, F9, F12, H8, H11, H14, K10, K13, L8, P8, R6, U8, V6, W10, Y8, AA6, AB10, AC8, AD12, AE10, AF8, AG12, AH10, AJ8, AJ14, AK12, AL10, AL16	SDRAM 1 I/O supply	D1_GV _{DD} 2.5- DDR 1.8 DDR2	
D2_GV _{DD}	B2, B5, B8, D4, D7, E2, F6, G4, H2, J6, K4, L2, M6, N4, P2, T4, U2, W4, Y2, AB4, AC2, AD6, AE4, AF2, AG6, AH4, AJ2, AK6, AL4, AM2	SDRAM 2 I/O supply	D2_GV _{DD} 2.5V - DDR 1.8V - DDR2	
OV _{DD}	B22, B25, B28, D17, D24, D27, F19, F22, F26, F29, G17, H21, H24, K19, K23, M21, AM30	DUART, Local Bus, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, JTAG, Power management, I ² C, JTAG and Miscellaneous I/O voltage	OV _{DD} 3.3V	
LV _{DD}	AC20, AD23, AH22	TSEC1 and TSEC2 I/O voltage	LV _{DD} 2.5/3.3V	
TV _{DD}	AC17, AG18, AK20	TSEC3 and TSEC4 I/O voltage	TV _{DD} 2.5/3.3V	
SV _{DD}	H31, J29, K28, K32, L30, M28, M31, N29, R30, T31, U29, V32, W30, Y31, AA29, AB32, AC30, AD31, AE29, AG30, AH31, AJ29, AK32, AL30, AM31	Transceiver Power Supply SerDes	SV _{DD} 1.05/1.1V	
XV _{DD-SRDS1}	K26, L24, M27, N25, P26, R24, R28, T27, U25, V26	Serial I/O Power Supply for SerDes Port 1	XV _{DD-SRDS1} 1.05/1.1V	
XV _{DD-SRDS2}	AA25, AB28, AC26, AD27, AE25, AF28, AH27, AK28, AM27, W24, Y27	Serial I/O Power Supply for SerDes Port 2	XV _{DD-SRDS2} 1.05/1.1V	
V _{DD-Core0}	L12, L13, L14, M13, M15, N12, N14, P11, P13, P15, R12, R14, T11, T13, T15, U12, U14, V11, V13, V15, W12, W14, Y12, Y13, Y15, AA12, AA14, AB13	Core 0 voltage supply	V _{DD-Core0} 1.05/1.1V	
V _{DD-Core1}	R16, R18, R20, T17, T19, T21, T23, U16, U18, U22, V17, V19, V21, V23, W16, W18, W20, W22, Y17, Y19, Y21, Y23, AA16, AA18, AA20, AA22, AB23, AC24	Core 1 voltage supply	V _{DD-Core1} 1.05/1.1V	(12) S1
V _{DD-PLAT}	M16, M17, M18, N16, N20, N22, P17, P19, P21, P23, R22	Platform supply voltage	V _{DD-PLAT} 1.05/1.1V	
AV _{DD-Core0}	B20	Core 0 PLL Supply	AV _{DD-Core0} 1.05/1.1V	
AV _{DD-Core1}	A19	Core 1 PLL Supply	AV _{DD-Core1} 1.05/1.1V	(12) S2

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Table 18-1. PC8641 Signal Reference by Functional Block (Continued)

Name ⁽¹⁾	Package Pin Number	Pin Type	Power Supply	Notes
AV _{DD} _PLAT	B19	Platform PLL supply voltage	AV _{DD} _PLAT 1.05/1.1V	
AV _{DD} _LB	A20	Local Bus PLL supply voltage	AV _{DD} _LB 1.05/1.1V	
AV _{DD} _SRDS1	P32	SerDes Port 1 PLL & DLL Power Supply	AV _{DD} _SRDS1 1.05/1.1V	
AV _{DD} _SRDS2	AF32	SerDes Port 2 PLL & DLL Power Supply	AV _{DD} _SRDS2 1.05/1.1V	
GND	C3, C6, C9, C12, C15, C23, C26, E5, E8, E11, E14, E18, E25, E28, F3, G7, G10, G13, G20, G23, G27, G30, H5, J3, J9, J12, J15, J22, J25, K7, L5, L20, M3, M9, M12, N7, N11, N13, N15, N17, N19, N21, N23, P5, P12, P16, P20, P22, R3, R9, R11, R13, R15, R17, R19, R21, R23, T7, T12, T14, T16, T18, T20, T22, U5, U11, U13, U15, U17, U19, U21, U23, V3, V9, V12, V14, V16, V18, V22, W7, W11, W13, W15, W17, W19, W21, W23, Y5, Y14, Y16, Y18, Y20, Y22, AA3, AA9, AA13, AA15, AA17, AA19, AA21, AA23, AB7, AB24, AC5, AC11, AD3, AD9, AD15, AE7, AE13, AE18, AF5, AF11, AF21, AF24, AG3, AG9, AH7, AH13, AJ5, AJ11, AK3, AK9, AK15, AK19, AK23, AL7, AL13	GND	–	
AGND_SRDS1	P30	SerDes Port 1 Ground pin for AV _{DD} _SRDS1	–	
AGND_SRDS2	AF30	SerDes Port 2 Ground pin for AV _{DD} _SRDS2	–	
SGND	H28, H32, J30, K31, L28, L29, M32, N30, R29, T32, U30, V31, W29, Y32 AA30, AB31, AC29, AD32, AE30, AG29, AH32, AJ30, AK31, AL29, AM32	Ground pins for SV _{DD}		
XGND	K27, L25, M26, N24, P27, R25, T26, U24, V27, W25, Y28, AA24, AB27, AC25, AD28, AE26, AF27, AH28, AJ26, AK27, AL26, AM28	Ground pins for XV _{DD} _SRDS _n		
Reset Configuration Signals⁽²⁰⁾				
TSEC1_TXD[0]/ cfg_alt_boot_vec	AF25	–	LV _{DD}	
TSEC1_TXD[1]/ cfg_platform_freq	AC23	–	LV _{DD}	(21)
TSEC1_TXD[2:4]/ cfg_device_id[5:7]	AG24, AG23, AE24	–	LV _{DD}	
TSEC1_TXD[5]/ cfg_tsec1_reduce	AE23	–	LV _{DD}	
TSEC1_TXD[6:7]/ cfg_tsec1_prctl[0:1]	AE22, AD22	–	LV _{DD}	
TSEC2_TXD[0:3]/ cfg_rom_loc[0:3]	AB20, AJ23, AJ22, AD19	–	LV _{DD}	
TSEC2_TXD[4], TSEC2_TX_ER/ cfg_dram_type[0:1]	AH23, AB19	–	LV _{DD}	(38)
TSEC2_TXD[5]/ cfg_tsec2_reduce	AH21	–	LV _{DD}	

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Table 18-1. PC8641 Signal Reference by Functional Block (Continued)

Name ⁽¹⁾	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_TXD[6:7]/ cfg_tsec2_prtcl[0:1]	AG22, AG21	–	LV _{DD}	
TSEC3_TXD[0:1]/ cfg_spare[0:1]	AL21, AJ21	O	TV _{DD}	(33)
TSEC3_TXD[2]/ cfg_core1_enable	AM20	O	TV _{DD}	
TSEC3_TXD[3]/ cfg_core1_lm_offset	AJ20	–	LV _{DD}	
TSEC3_TXD[5]/ cfg_tsec3_reduce	AK21	–	LV _{DD}	
TSEC3_TXD[6:7]/ cfg_tsec3_prtcl[0:1]	AL20, AL19	–	LV _{DD}	
TSEC4_TXD[0:3]/ cfg_io_ports[0:3]	AC18, AC16, AD18, AD17	–	LV _{DD}	
TSEC4_TXD[5]/ cfg_tsec4_reduce	AB18	–	LV _{DD}	
TSEC4_TXD[6:7]/ cfg_tsec4_prtcl[0:1]	AB17, AB16	–	LV _{DD}	
LAD[0:31]/ cfg_gpporcr[0:31]	A30, E29, C29, D28, D29, H25, B29, A29, C28, L22, M22, A28, C27, H26, G26, B27, B26, A27, E27, G25, D26, E26, G24, F27, A26, A25, C25, H23, K22, D25, F25, H22	–	OV _{DD}	
$\overline{\text{LWE}}[0]$ /cfg_cpu_boot	E21	–	OV _{DD}	
$\overline{\text{LWE}}[1]$ /cfg_rio_sys_size	F21	–	OV _{DD}	
$\overline{\text{LWE}}[2:3]$ / cfg_host_agt[0:1]	D22, E20	–	OV _{DD}	
LDP[0:3], LA[27]/ cfg_core_pll[0:4]	A24, E24, C24, B24, J21	–	OV _{DD}	(22)
LA[28:31]/ cfg_sys_pll[0:3]	K21, G22, F24, G21	–	OV _{DD}	(22)
LGPL[3], LGPL[5]/ cfg_boot_seq[0:1]	K20, J19	–	OV _{DD}	
D1_MSRCID[0]/ cfg_mem_debug	F15	–	OV _{DD}	
D1_MSRCID[1]/ cfg_ddr_debug	K15	–	OV _{DD}	

- Notes:
- Multi-pin signals such as D1_MDQ[0:63] and D2_MDQ[0:63] have their physical package pin numbers listed in order corresponding to the signal names.
 - Stub Series Terminated Logic (SSTL-18 and SSTL-25) type pins.
 - If a DDR port is not used, it is possible to leave the related power supply (Dn_GV_{DD}, Dn_MV_{REF}) turned off at reset. Note that these power supplies can only be powered up again at reset for functionality to occur on the DDR port.
 - Low Voltage Differential Signaling (LVDS) type pins.
 - Low Voltage Transistor-Transistor Logic (LVTTL) type pins.
 - This pin is a reset configuration pin and appears again in the Reset Configuration Signals section of this table. See the Reset Configuration Signals section of this table for config name and connection details.
 - Recommend a weak pull-up resistor (2–10 k Ω) be placed from this pin to its power supply.
 - Recommend a weak pull-down resistor (2–10 k Ω) be placed from this pin to ground.

9. This multiplexed pin has input status in one mode and output in another.
10. This pin is a multiplexed signal for different functional blocks and appears more than once in this table.
11. This pin is open drain signal.
12. Functional only on the PC8641D.
13. These pins should be left floating.
14. These pins should be connected to SV_{DD} .
15. These pins should be pulled to ground with a strong resistor (270- Ω to 330- Ω).
16. These pins should be connected to OV_{DD} .
17. This is a SerDes PLL/DLL digital test signal and is only for factory use.
18. This is a SerDes PLL/DLL analog test signal and is only for factory use.
19. This pin should be pulled to ground with a 100 Ω resistor.
20. The pins in this section are reset configuration pins. Each pin has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-k Ω pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
21. Should be pulled down at reset if platform frequency is at 400 MHz.
22. These pins require 4.7-k Ω pull-up or pull-down resistors and must be driven as they are used to determine PLL configuration ratios at reset.
23. This output is actively driven during reset rather than being tri-stated during reset.
24. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
25. This pin should NOT be pulled down (or driven low) during reset.
26. These are test signals for factory use only and must be pulled up (100 Ω to 1 k Ω) to OV_{DD} for normal machine operation.
27. Dn_MDIC[0] should be connected to ground with an 18 Ω resistor $\pm 1\Omega$ and Dn_MDIC[1] should be connected to $Dn_{GV_{DD}}$.
28. Pin N18 is recommended as a reference point for determining the voltage of V_{DD_PLAT} and is hence considered as the V_{DD_PLAT} sensing voltage and is called SENSEV $_{DD_PLAT}$.
29. Pin P18 is recommended as the ground reference point for SENSEV $_{DD_PLAT}$ and is called SENSEVSS_PLAT.
30. This pin should be pulled to ground with a 200 Ω resistor.
31. These pins are connected to the power/ground planes internally and may be used by the core power supply to improve tracking and regulation.
32. Must be tied low if unused.
33. These pins may be used as defined functional reset configuration pins in the future. Please include a resistor pull up/down option to allow flexibility of future designs.
34. Used as serial data output for SRIO 1x/4x link.
35. Used as serial data input for SRIO 1x/4x link.
36. This pin requires an external 4.7 k Ω pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
37. This pin is only an output in FIFO mode when used as Rx Flow Control.
38. This pin functions as `cfg_dram_type[0 or 1]` at reset and MUST BE VALID BEFORE HRESET ASSERTION in device sleep mode.
39. Should be pulled to ground if unused (such as in FIFO, MII and RMII modes).
40. See [Section 19.4.2 "Platform to FIFO restrictions"](#) on page 89 for clock speed limitations for this pin when used in FIFO mode.
41. The phase between the output clocks TSEC1_GTX_CLK and TSEC2_GTX_CLK (ports 1 and 2) is no more than 100 ps. The phase between the output clocks TSEC3_GTX_CLK and TSEC4_GTX_CLK (ports 3 and 4) is no more than 100 ps.
42. For systems which boot from Local Bus (GPCM)-controlled flash, a pullup on LGPL4 is required.

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Special Notes for Single Core Device:

S1. Solder ball for this signal will not be populated in the single core package.

S2. The PLL filter from V_{DD_Core1} to AV_{DD_Core1} should be removed. AV_{DD_Core1} should be pulled to ground with a weak (2–10 k Ω) resistor. See [Section 21.2.1 "PLL Power Supply Filtering" on page 96](#) for more details.

S3. This pin should be pulled to GND for the single core device.

S4. No special requirement for this pin on single core device. Pin should be tied to power supply as directed for dual core.

19. Clocking

This section describes the PLL configuration of the PC8641. Note that the platform clock is identical to the MPX clock.

19.1 Clock Ranges

[Table 19-1](#) provides the clocking specifications for the processor cores and [Table 19-2](#) provides the clocking specifications for the memory bus.

Table 19-1. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency								Unit	Notes
	1000 MHz		1250 MHz		1333 MHz		1500 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	800	1000	800	1250	800	1333	800	1500	MHz	(1)(2)

Notes: 1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 19.2 "MPX to SYSCLK PLL Ratio" on page 87](#) and [Section 19.3 "e600 to MPX clock PLL Ratio" on page 88](#), for ratio settings.

2. The minimum e600 core frequency is based on the minimum platform clock frequency of 400 MHz.

Table 19-2. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	1000, 1250, 1333, 1500 MHz			
	Min	Max		
Memory bus clock frequency	200	300	MHz	(1)(2)

Notes: 1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 19.2 "MPX to SYSCLK PLL Ratio" on page 87](#).

2. The memory bus clock speed is half the DDR/DDR2 data rate, hence, half the MPX clock frequency.

Table 19-3. Platform/MPX Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	1000, 1250, 1333, 1500 MHz			
	Min	Max		
Platform/MPX bus clock frequency	400	500-600	MHz	(1)(2)

- Notes:
- Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to [Section 19.2 "MPX to SYSCLK PLL Ratio" on page 87](#) and [Section 19.3 "e600 to MPX clock PLL Ratio" on page 88](#) for ratio settings.
 - Platform/MPX frequencies between 400 and 500 MHz are not supported.

Table 19-4. Local Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	1000, 1250, 1333, 1500 MHz			
	Min	Max		
Local bus clock speed (for Local Bus Controller)	25	133	MHz	(1)

- Note:
- The Local bus clock speed on LCLK[0:2] is determined by MPX clock divided by the Local Bus PLL ratio programmed in LCCR[CLKDIV]. See the reference manual for the PC8641D for more information on this.

19.2 MPX to SYSCLK PLL Ratio

The MPX clock is the clock that drives the MPX bus, and is also called the platform clock. The frequency of the MPX is set using the following reset signals, as shown in [Table 19-5](#):

- SYSCLK input signal
- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the MPX bus frequency, since the MPX frequency must equal the DDR data rate.

Table 19-5. MPX:SYSCLK Ratio

Binary Value of LA[28:31] Signals	MPX:SYSCLK Ratio
0000	Reserved
0001	Reserved
0010	2:1
0011	3:1
0100	4:1
0101	5:1
0110	6:1
0111	Reserved
1000	8:1
1001	9:1

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19.3 e600 to MPX clock PLL Ratio

Table 19-6 describes the clock ratio between the platform and the e600 core clock. This ratio is determined by the binary value of LDP[0:3], LA[27](cfg_core_pll[0:4] - reset config name) at power up, as shown in Table 19-6.

Table 19-6. e600 Core to MPX Clock Ratio

Binary Value of LDP[0:3], LA[27] Signals	e600 core:MPX Clock Ratio
01000	2:1
01100	2.5:1
10000	3:1
11100	3.5:1
10100	4:1
01110	4.5:1

19.4 Frequency Options

19.4.1 Sysclk to Platform Frequency Options

Table 19-7 shows some SYSCLK frequencies and the expected MPX frequency values based on the MPX clock to SYSCLK ratio. Note that frequencies between 400 MHz and 500 MHz are NOT supported on the platform. See note regarding cfg_platform_freq in Section 18. "Signal Listings" on page 75 since it is a reset configuration pin that is related to platform frequency.

Table 19-7. Frequency Options of SYSCLK with Respect to Platform/MPX Clock Speed

MPX to SYSCLK Ratio	SYSCLK (MHz)																							
	66	83	100	111	133	167																		
	Platform/MPX Frequency (MHz) ⁽¹⁾																							
2																								
3																								
4																								
5																								
6																								
8																								
9																								
													400	500	600	555	400	500						
													533				533							
													600											

Note: 1. SYSCLK frequency range is 66-168 MHz. Platform clock/ MPX frequency range is 400 MHz, 500-600 MHz.

19.4.2 Platform to FIFO restrictions

Please note the following FIFO maximum speed restrictions based on platform speed.

For FIFO GMII mode:

FIFO TX/RX clock frequency \leq platform clock frequency / 4.2

For example, if the platform frequency is 533MHz, the FIFO TX/RX clock frequency should be no more than 127 MHz

For FIFO encoded mode:

FIFO TX/RX clock frequency \leq platform clock frequency / 3.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz

20. Thermal

This section describes the thermal specifications of the PC8641.

20.1 Thermal Characteristics

Table 20-1 provides the package thermal characteristics for the PC8641.

Table 20-1. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient thermal resistance, natural convection, single-layer (1s) board	$R_{\theta JA}$	18	$^{\circ}C/W$	(1)(2)
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JA}$	13	$^{\circ}C/W$	(1)(3)
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	$R_{\theta JMA}$	13	$^{\circ}C/W$	(1)(3)
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	$R_{\theta JMA}$	9	$^{\circ}C/W$	(1)(3)
Junction-to-board thermal resistance	$R_{\theta JB}$	5	$^{\circ}C/W$	(4)
Junction-to-case thermal resistance	$R_{\theta JC}$	< 0.1	$^{\circ}C/W$	(5)

- Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
 2. Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
 3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
 4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
 5. This is the thermal resistance between die and case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. Actual thermal resistance is less than 0.1 $^{\circ}C/W$.

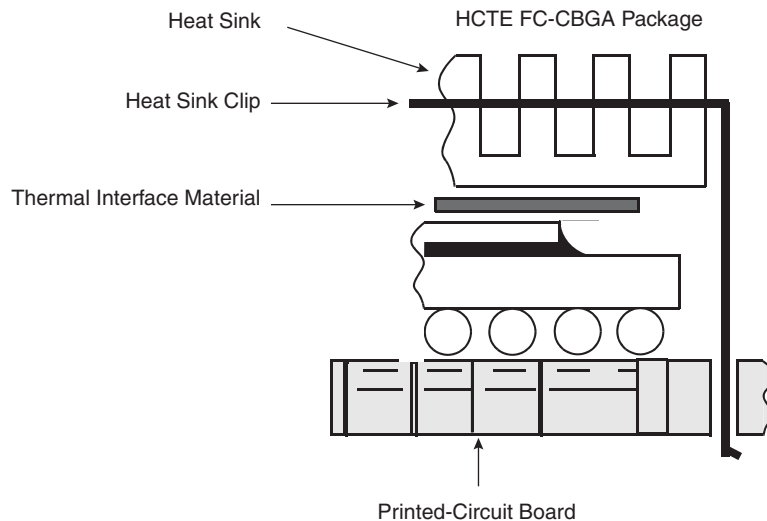
Note: The thermal performance of the LGA and the BGA versions of the package are the same. For the thermal model, the only difference is the height of the solder layer under the substrate.

20.2 Thermal Management Information

This section provides thermal management information for the high coefficient of thermal expansion (HiTCE) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design: the heat sink, airflow, and thermal interface material. The PC8641 implements several features designed to assist with thermal management, including the temperature diode. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see [Section 20.2.4 "Temperature Diode" on page 94](#), for more information.

To reduce the die-junction temperature, heat sinks are required; due to the potential large mass of the heat sink, attachment through the printed-circuit board is suggested. In any implementation of a heat sink solution, the force on the die should not exceed ten pounds force (45 newtons). [Figure 20-1](#) and [Figure 20-2 on page 91](#) show a spring clip through the board. Occasionally the spring clip is attached to soldered hooks or to a plastic backing structure. Screw and spring arrangements are also frequently used.

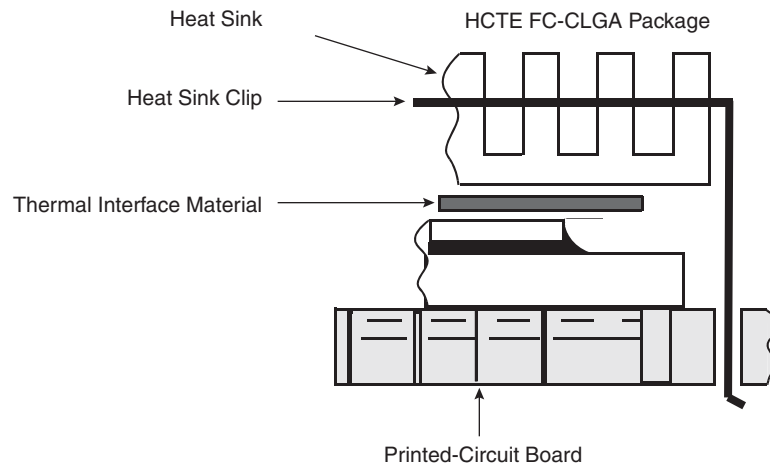
Figure 20-1. FC-CBGA Package Exploded Cross-Sectional View with Several Heat Sink Options



A clip-on-chip heat sink solution will NOT work with the FC-CLGA part.

A through-hole solution is recommended, as shown in [Figure 20-2 on page 91](#) below.

Figure 20-2. FC-CLGA Package Exploded Cross-Sectional View with Several Heat Sink Options



Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

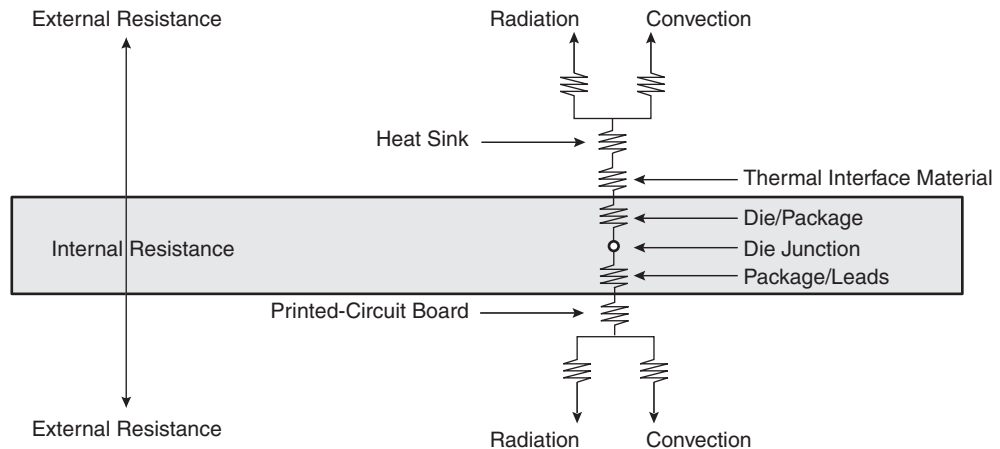
20.2.1 Internal Package Conduction Resistance

For the exposed-die packaging technology described in [Table 20-1 on page 89](#), the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance (the case is actually the top of the exposed silicon die)
- The die junction-to-board thermal resistance

[Figure 20-3](#) depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Figure 20-3. Package with Heat Sink Mounted to a Printed-Circuit Board



Heat generated on the active side of the chip is conducted through the silicon, through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

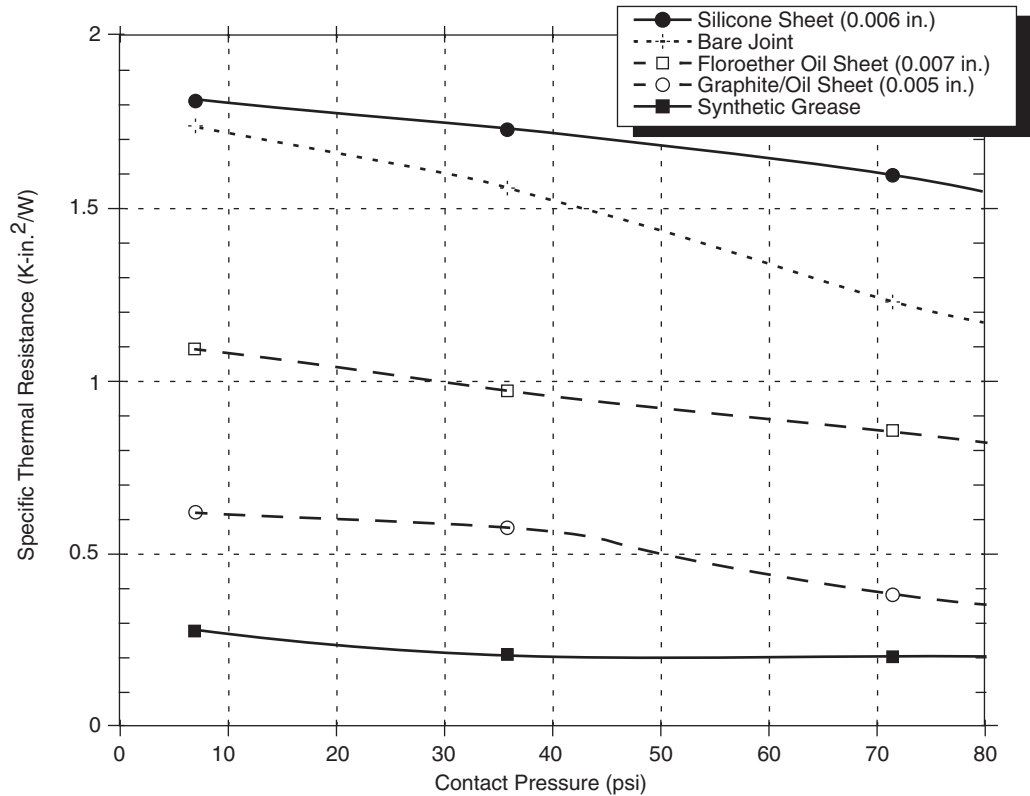
Because the silicon thermal resistance is quite small, the temperature drop in the silicon may be neglected for a first-order analysis. Thus the thermal interface material and the heat sink conduction/conductive thermal resistances are the dominant terms.

20.2.2 Thermal Interface Materials

A thermal interface material is recommended at the package-to-heat sink interface to minimize the thermal contact resistance. Figure 20-4 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 20-1 on page 90). Therefore, synthetic grease offers the best thermal performance, considering the low interface pressure, and is recommended due to the high power dissipation of the PC8641. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.

Figure 20-4. Thermal Performance of Select Thermal Interface Materials



20.2.3 Heat Sink Selection Example

The following section provides a heat sink selection example using one of the commercially available heat sinks.

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_J = T_I + T_R + (R_{\theta JC} + R_{\theta INT} + R_{\theta SA}) \times P_D$$

where

T_J is the die-junction temperature

T_i is the inlet cabinet ambient temperature

T_R is the air temperature rise within the computer cabinet

$R_{\theta_{JC}}$ is the junction-to-case thermal resistance

$R_{\theta_{INT}}$ is the adhesive or interface material thermal resistance

$R_{\theta_{SA}}$ is the heat sink base-to-ambient thermal resistance

P_D is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in [Table 3-2 on page 7](#). The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_i) may range from 30° to 40° C. The air temperature rise within a cabinet (T_R) may be in the range of 5° to 10° C. The thermal resistance of the thermal interface material ($R_{\theta_{INT}}$) is typically about 0.2° C/W. For example, assuming a T_i of 30° C, a T_R of 5° C, a package $R_{\theta_{JC}} = 0.1$, and a typical power consumption (P_D) of 43.4 W, the following expression for T_j is obtained:

$$\text{Die-junction temperature: } T_j = 30^\circ \text{ C} + 5^\circ \text{ C} + (0.1^\circ \text{ C/W} + 0.2^\circ \text{ C/W} + \theta_{sa}) \times 43.4 \text{ W}$$

For this example, a $R_{\theta_{sa}}$ value of 1.32° C/W or less is required to maintain the die junction temperature below the maximum value of [Table 3-2](#).

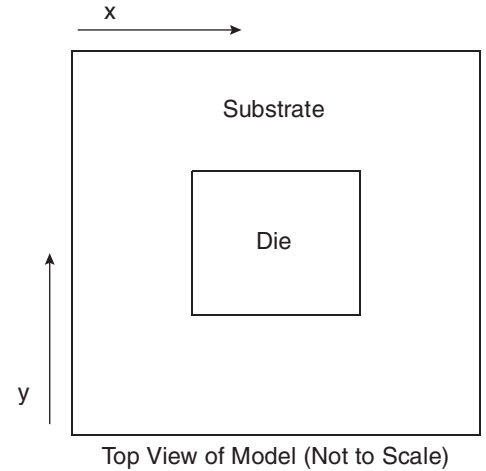
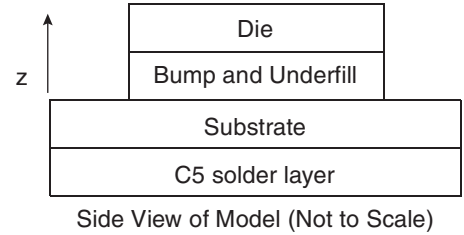
Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, and so on.

Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs.

For system thermal modeling, the PC8641 thermal model is shown in [Figure 20-5 on page 94](#). Four cuboids are used to represent this device. The die is modeled as 12.4x15.3 mm at a thickness of 0.86 mm. See [Section 4. "Power Characteristics" on page 12](#) for power dissipation details. The substrate is modeled as a single block 33x33x1.2 mm with orthotropic conductivity: 13.5 W/(m • K) in the xy-plane and 5.3 W/(m • K) in the z-direction. The die is centered on the substrate. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate with a conductivity of 5.3 W/(m • K) in the thickness dimension of 0.07 mm. Because the bump/underfill is modeled with zero physical dimension (collapsed height), the die thickness was slightly enlarged to provide the correct height. The C5 solder layer is modeled as a cuboid with dimensions 33x33x0.4 mm and orthotropic thermal conductivity of 0.034 W/(m • K) in the xy-plane and 9.6 W/(m • K) in the z-direction. An LGA solder layer would be modeled as a collapsed thermal resistance with thermal conductivity of 9.6W/(m • K) and an effective height of 0.1 mm. The thermal model uses approximate dimensions to reduce grid. Please refer to the case outline for actual dimensions.

Figure 20-5. Recommended Thermal Model of PC8641

Conductivity	Value	Unit
Die (12.4 x 15.3 x 0.86 mm)		
Silicon	Temperature dependent	
Bump and Underfill (12.4 x 15.3 x 0.07 mm) Collapsed Resistance		
k_z	5.3	W/(m x K)
Substrate (33 x 33 x 1.2 mm)		
k_x	13.5	W/(m x K)
k_y	13.5	
k_z	5.3	
C5 Solder layer (33 x 33 x 0.4 mm)		
k_x	0.034	W/(m x K)
k_y	0.034	
k_z	9.6	



20.2.4 Temperature Diode

The PC8641 has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. For proper operation, the monitoring device used should auto-calibrate the device by canceling out the V_{BE} variation of each PC8641's internal diode.

The following are the specifications of the PC8641 on-board temperature diode:

$V_f > 0.40V$

$V_f < 0.90V$

Operating range 2-300 μA

Diode leakage < 10 nA at 125°C

Ideality factor over 5-150 μA at 60°C: $n = 1.0275 \pm 0.9\%$

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_S \left[e^{\frac{qV_f}{nKT}} - 1 \right]$$

Another useful equation is:

$$V_H - V_L = n \frac{KT}{q} \left[\frac{I_H}{I_L} \right]$$

Where:

I_{fw} = Forward current

I_s = Saturation current

V_d = Voltage at diode

V_f = Voltage forward biased

V_H = Diode voltage while I_H is flowing

V_L = Diode voltage while I_L is flowing

I_H = Larger diode bias current

I_L = Smaller diode bias current

q = Charge of electron (1.6×10^{-19} C)

n = Ideality factor (normally 1.0)

K = Boltzman's constant (1.38×10^{-23} Joules/K)

T = Temperature (Kelvins)

The ratio of I_H to I_L is usually selected to be 10:1. The above simplifies to the following:

$$V_H - V_L = 1.986 \times 10^{-4} \times nT$$

Solving for T , the equation becomes:

$$nT = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

21. System Design Information

This section provides electrical and thermal design recommendations for successful application of the PC8641.

21.1 System Clocking

This device includes six PLLs, as follows:

1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in [Section 19.2 "MPX to SYSCLK PLL Ratio" on page 87](#).
2. The dual e600 Core PLLs generate the e600 clock from the externally supplied input.
3. The local bus PLL generates the clock for the local bus.
4. There are two internal PLLs for the SerDes block.

21.2 Power Supply Design and Sequencing

21.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in [Figure 21-2](#), one to each of the AV_{DD} type pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} type pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} type pin, which is on the periphery of the footprint, without the inductance of vias.

[Figure 21-1](#) and [Figure 21-2](#) show the PLL power supply filter circuits for the platform and cores, respectively.

Figure 21-1. PC8641 PLL Power Supply Filter Circuit (for platform and Local bus)

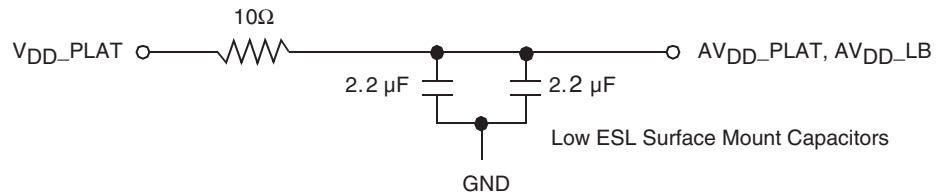
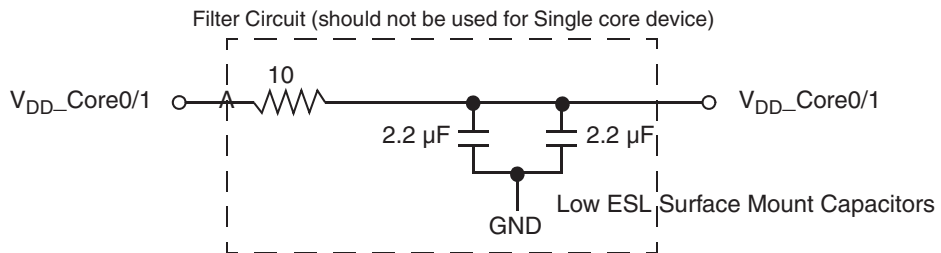


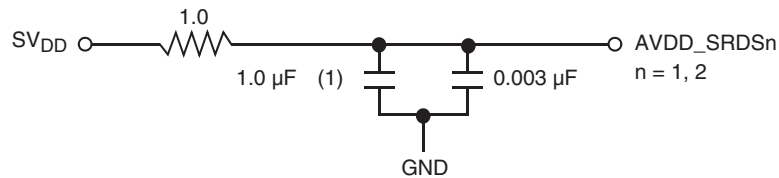
Figure 21-2. PC8641 PLL Power Supply Filter Circuit (for cores)



Note: For single core device the filter circuit (in the dashed box) should be removed and AV_{DD}_Core1 should be tied to ground with a weak (2-10 kΩ) pull-down resistor.

The AV_{DD}_SRDSn signals provide power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDSn balls to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SRDSn balls. The 0.003-μF capacitor is closest to the balls, followed by the 1-μF capacitor, and finally the 1 ohm resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDSn to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.

Figure 21-3. SerDes PLL Power Supply Filter



Note: 1. An 0805 sized capacitor is recommended for system initial bring-up.

Note the following:

- AV_{DD} should be a filtered version of SV_{DD} .
- Signals on the SerDes interface are fed from the SV_{DD} power plan.

21.2.2 PLL Power Supply Sequencing

For details on power sequencing for the AV_{DD} type and supplies refer to [Section 3.2 "Power Up/Down Sequence"](#) on page 10

21.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads.

This noise must be prevented from reaching other components in the PC8641 system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each OV_{DD} , Dn_GV_{DD} , LV_{DD} , TV_{DD} , V_{DD_Coren} , and V_{DD_PLAT} pin of the device. These decoupling capacitors should receive their power from separate OV_{DD} , Dn_GV_{DD} , LV_{DD} , TV_{DD} , V_{DD_Coren} , and V_{DD_PLAT} and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μF . Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the OV_{DD} , Dn_GV_{DD} , LV_{DD} , TV_{DD} , V_{DD_Coren} , and V_{DD_PLAT} planes, to enable quick recharging of the smaller chip capacitors. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μF (AVX TPS tantalum or Sanyo OSCON).

21.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD_SRDSn}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 x 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1- μ F ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a 10- μ F, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100- μ F, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

21.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. In general all unused active low inputs should be tied to OV_{DD} , Dn_GV_{DD} , LV_{DD} , TV_{DD} , V_{DD_Coren} , and V_{DD_PLAT} , XV_{DD_SRDSn} , and SV_{DD} as required and unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Special cases:

DDR - If one of the DDR ports is not being used the power supply pins for that port can be connected to ground so that there is no need to connect the individual unused inputs of that port to ground. Note that these power supplies can only be powered up again at reset for functionality to occur on the DDR port.

Power supplies for other functional buses should remain powered.

Local Bus - If parity is not used, tie $LDP[0:3]$ to ground via a 4.7 k Ω resistor, tie $LPBSE$ to OV_{DD} via a 4.7 k Ω resistor (pull-up resistor).

SerDes - Receiver lanes configured for PCI Express are allowed to be disconnected (as would occur when a PCI Express slot is connected but not populated). Directions for terminating the SerDes signals is discussed in [Section 21.5.1 "Guidelines for High-Speed Interface Termination" on page 98](#).

21.5.1 Guidelines for High-Speed Interface Termination

21.5.1.1 SerDes Interface

The high-speed SerDes interface can be disabled through the POR input $cfg_io_ports[0:3]$ and through the $DEVDISR$ register in software. If a SerDes port is disabled through the POR input the user can not enable it through the $DEVDISR$ register in software. However, if a SerDes port is enabled through the POR input the user can disable it through the $DEVDISR$ register in software. Disabling a SerDes port through software should be done on a temporary basis. Power is always required for the SerDes interface, even if the port is disabled through either mechanism. [Table 21-1](#) describes the possible enabled/disabled scenarios for a SerDes port. The termination recommendations must be followed for each port.

Table 21-1. SerDes Port Enabled/Disabled Configurations

	Disabled through POR input	Enabled through POR input
Enabled through DEVDISR	SerDes port is disabled (and cannot be enabled through DEVDISR) Complete termination required (Reference Clock not required)	SerDes port is enabled Partial termination may be required ⁽¹⁾ (Reference Clock is required)
Disabled through DEVDISR	SerDes port is disabled (through POR input) Complete termination required (Reference Clock not required)	SerDes port is disabled after software disables port Same termination requirements as when the port is enabled through POR input ⁽²⁾ (Reference Clock is required)

- Notes:
1. Partial Termination when a SerDes port is enabled through both POR input and DEVDISR is determined by the SerDes port mode. If the port is in x8 PCI Express mode, no termination is required because all pins are being used. If the port is in x1/x2/x4 PCI Express mode, termination is required on the unused pins. If the port is in x4 Serial RapidIO mode termination is required on the unused pins.
 2. If a SerDes port is enabled through the POR input and then disabled through DEVDISR, no hardware changes are required. Termination of the SerDes port should follow what is required when the port is enabled through both POR input and DEVDISR. See Note⁽¹⁾ for more information.

If the high-speed SerDes port requires complete or partial termination, the unused pins should be terminated as described in this section.

The following pins must be left unconnected (floating):

- $SDn_TX[7:0]$
- $\overline{SDn_TX}[7:0]$

The following pins must be connected to GND:

- $SDn_RX[7:0]$
- $\overline{SDn_RX}[7:0]$
- SDn_REF_CLK
- $\overline{SDn_REF_CLK}$

Note: It is recommended to power down the unused lane through SRDS1CR1[0:7] register (offset = 0xE_0F08) and SRDS2CR1[0:7] register (offset = 0xE_0F44.) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

For other directions on reserved or no-connects pins see [Section 18. "Signal Listings" on page 75.](#)

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21.6 Pull-Up and Pull-Down Resistor Requirements

The PC8641 requires weak pull-up resistors (2–10 kΩ is recommended) on all open drain type pins.

The following pins must NOT be pulled down during power-on reset: TSEC4_TXD[4], LGPL0/LSDA10, LGPL1/LSDWE, TRIG_OUT/READY, and D1_MSRCID[2].

The following are factory test pins and require strong pull up resistors (100Ω –1 kΩ) to OV_{DD} [LSSD_MODE, TEST_MODE[0:3]]. The following pins require weak pull up resistors (2–10 kΩ) to their specific power supplies: $\overline{LCS}[0:4]$, $\overline{LCS}[5]/\overline{DMA_DREQ2}$, $\overline{LCS}[6]/\overline{DMA_DACK}[2]$, $\overline{LCS}[7]/\overline{DMA_DDONE}[2]$, IRQ_OUT, IIC1_SDA, IIC1_SCL, IIC2_SDA, IIC2_SCL, and $\overline{CKSTP_OUT}$.

The following pins should be pulled to ground with a 100Ω resistor: SD1_IMP_CAL_TX, SD2_IMP_CAL_TX. The following pins should be pulled to ground with a 200Ω resistor: SD1_IMP_CAL_RX, SD2_IMP_CAL_RX.

TSECN_TX_EN signals require an external 4.7-kΩ resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.

When the platform frequency is 400 MHz, TSEC1_TXD[1] must be pulled down at reset.

TSEC2_TXD[4] and TSEC2_TX_ER pins function as `cfg_dram_type[0 or 1]` at reset and MUST BE VALID BEFORE HRESET ASSERTION when coming out of device sleep mode.

21.6.1 Special instructions for Single Core device

The mechanical drawing for the single core device does not have all the solder balls that exist on the single core device. This includes all the balls for V_{DD_Core1} and $SENSEV_{DD_Core1}$ which exist on the package for the dual core device, but not on the single core package. A solder ball is present for $SENSEV_{SS_Core1}$ and needs to be connected to ground with a weak (2-10 kΩ) pull down resistor. Likewise, AV_{DD_Core1} needs to be pulled to ground as shown in [Figure 21-2 on page 96](#).

The mechanical drawing for the single core device is located in [Section 17.2 "Mechanical Dimensions of the PC8641 FC-CBGA" on page 73](#).

For other pin pull-up or pull-down recommendations of signals, please see [Section 18. "Signal Listings" on page 75](#).

21.7 Output Buffer DC Impedance

The PC8641 drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I²C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see [Figure 21-4 on page 101](#)). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices.

When data is held high, SW1 is closed (SW2 is open) and R_p is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_p then becomes the resistance of the pull-up devices. R_p and R_N are designed to be close to each other in value. Then, $Z_0 = (R_p + R_N)/2$.

Figure 21-4. Driver Impedance Measurement

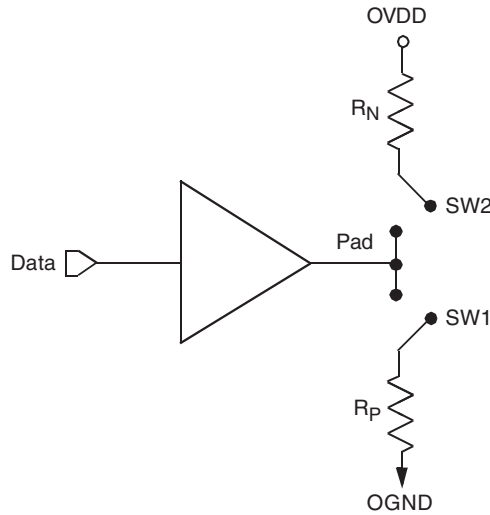


Table 21-2 summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD} , nominal OV_{DD} , $110^{\circ}C$.

Table 21-2. Impedance Characteristics

Impedance	DUART, Control, Configuration, Power Management	PCI Express	DDR DRAM	Symbol	Unit
R_N	43 Target	25 Target	20 Target	Z_0	W
R_P	43 Target	25 Target	20 Target	Z_0	W

Note: Nominal supply voltages. See Table 3-1 on page 6, $T_J = 110^{\circ}C$

21.8 Configuration Pin Muxing

The PC8641 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While \overline{HRESET} is asserted however, these pins are treated as inputs. The value presented on these pins while \overline{HRESET} is asserted, is latched when \overline{HRESET} deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during \overline{HRESET} (and for platform /system clocks after \overline{HRESET} deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e600 PLL ratio configuration pins are not equipped with these default pull-up devices.

21.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in [Figure 21-6 on page 104](#). Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP port connects primarily through the JTAG interface of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in [Figure 21-5 on page 103](#) allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in [Figure 21-5](#), for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header shown in [Figure 21-5](#); consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in [Figure 21-5](#) is common to all known emulators.

For a multi-processor non-daisy chain configuration, [Figure 21-6](#), can be duplicated for each processor. The recommended daisy chain configuration is shown in [Figure 21-7 on page 105](#). Please consult with your tool vendor to determine which configuration is supported by their emulator.

21.9.1 Termination of Unusual Signals

If the JTAG interface and COP header will not be used, e2v recommends the following connections:

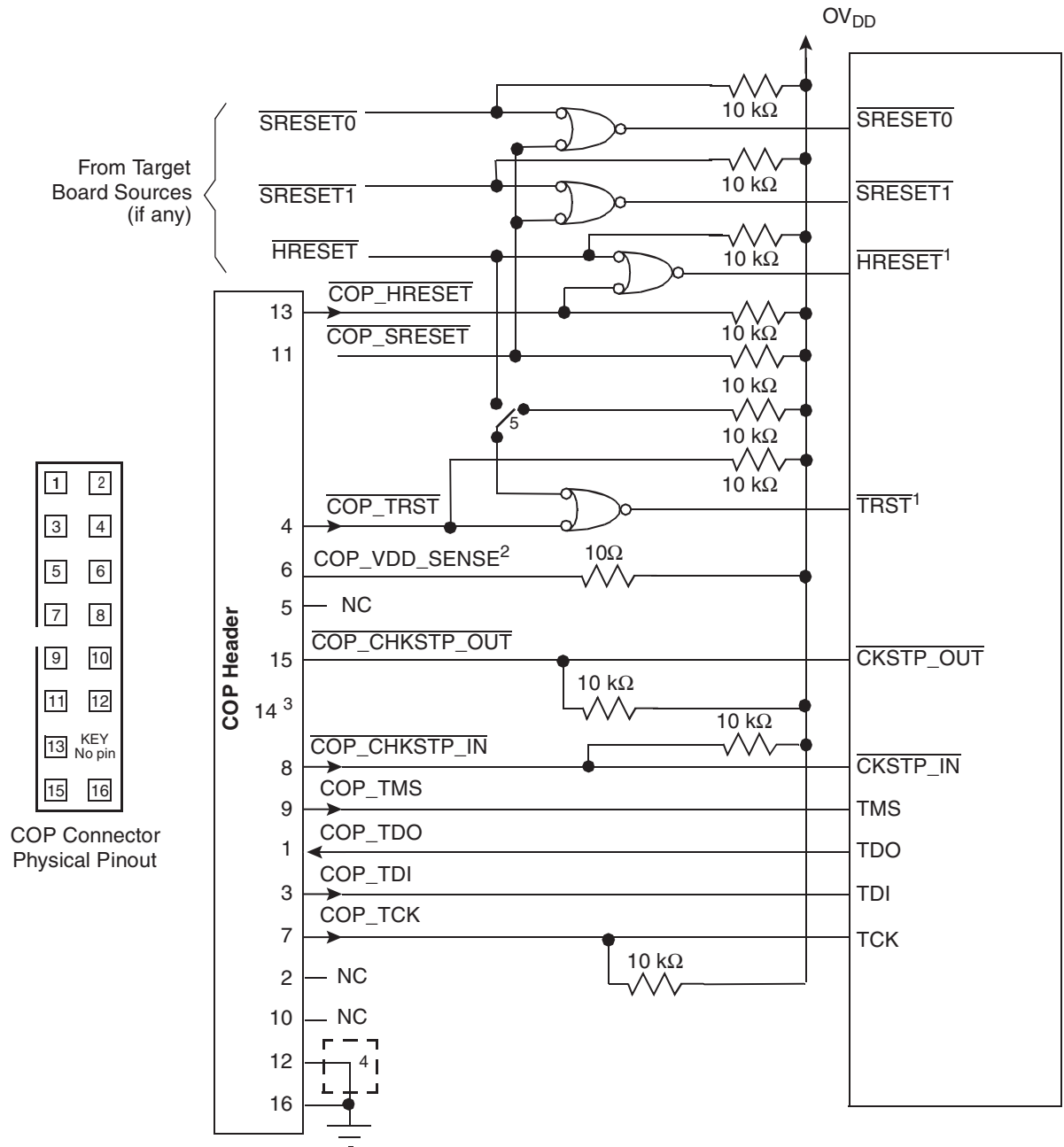
- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 k Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. e2v recommends that the COP header be designed into the system as shown in [Figure 21-6 on page 104](#). If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10 k Ω resistor. This will prevent TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.

Figure 21-5. COP Connector Physical Pinout

COP_TDO	1	2	NC
COP_TDI	3	4	$\overline{\text{COP_TRST}}$
NC	5	6	COP_VDD_SENSE
COP_TCK	7	8	$\overline{\text{COP_CHKSTP_IN}}$
COP_TMS	9	10	NC
$\overline{\text{COP_SRESET}}$	11	12	NC
$\overline{\text{COP_HRESET}}$	13	KEY No pin	
$\overline{\text{COP_CHKSTP_OUT}}$	15	16	GND

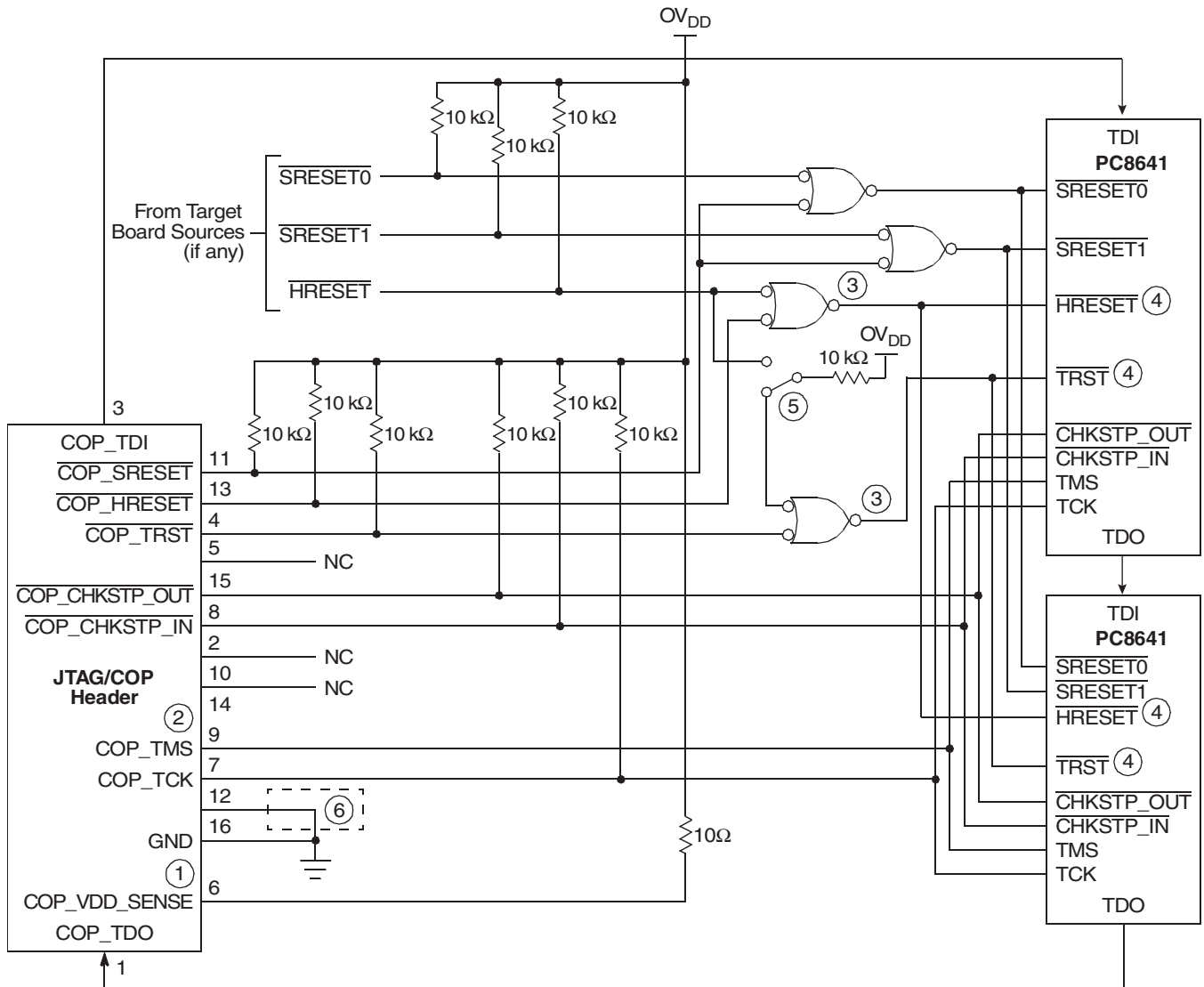
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Figure 21-6. JTAG/COP Interface Connection for one PC8641 device



- Notes:
1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
 2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
 3. The KEY location (pin 14) is not physically present on the COP header.
 4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
 5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.

Figure 21-7. JTAG/COP Interface Connection for multiple PC8641 devices in daisy chain configuration



- Notes:
1. Populate this with a 10Ω resistor for short circuit/current-limiting protection.
 2. KEY location; pin 14 is not physically present on the COP header.
 3. Use a AND gate with sufficient drive strength to drive two inputs.
 4. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown above.
 5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.
 6. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.

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22. Ordering Information

Ordering information for the parts fully covered by this specification document is provided in [Section 22.1 "Part Numbers Fully Addressed by This Document"](#).

22.1 Part Numbers Fully Addressed by This Document

[Figure 22-1](#) provides the e2v part numbering nomenclature for the PC8641. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local e2v. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Figure 22-1. Ordering Information

Product Code ⁽¹⁾	Part Identifier	Core Count	Temperature Range ⁽¹⁾	Package ⁽¹⁾	Core Processor Frequency ⁽³⁾ (MHz)	DDR speed (MHz)	Revision Level ⁽¹⁾
PC(X) ⁽²⁾	8641	Blank = Single Core D = Dual core	V: T _C = -40°C, T _J = +110°C M: T _C = -55°C, T _J = +125°C	GH = HiTCE FC-CBGA SH = RoHS HiTCE FC-CBGA	1000, 1250, 1333, 1500	N = 500 MHz ⁽⁴⁾ K = 600 MHz J = 533 MHz H = 500 MHz G = 400 MHz	Revision B = 2.0 System Version Register Value for Rev B: 0x8090_0020 - PC8641 0x8090_0120 - PC8641D Revision C = 2.1 System Version Register Value for Rev C: 0x8090_0021 - PC8641 0x8090_0121 - PC8641D Revision E = 3.0 System Version Register Value for Rev E: 0x8090_0030 - PC8641 0x8090_0130 - PC8641D

- Notes:
- For availability of the different versions, contact your local e2v sales office.
 - The letter X in the part number designates a "Prototype" product that has not been qualified by e2v. Reliability of a PCX part number is not guaranteed and such part-number shall not be used in Flight Hardware. Product changes may still occur while shipping prototypes.
 - Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
 - Part Number PC8641xxx1000NX is our low V_{DD_Core}n device. V_{DD_Core}n = 0.95V and V_{DD_PLAT} = 1.05V.

23. Definitions

23.1 Life Support Applications

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. e2v customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify e2v for any damages resulting from such improper use or sale.

24. Document Revision History

Table 24-1 provides a revision history for this hardware specification.

Table 24-1. Document Revision History

Rev. No	Date	Substantive Change(s)
0893C	01/2010	<ul style="list-style-type: none"> - Updated Table 4-1 on page 12 and Table 4-3 on page 14 : Added TBC for maximum power consumption at $t_j = 125^\circ\text{C}$ - Added note ⁽⁸⁾ to Table 15-2 on page 56 - Added Revision E to Figure 22-1 "Ordering Information" on page 106
0893B	12/2008	<ul style="list-style-type: none"> - Added Section 5.4 "Platform Frequency Requirements for PCI-Express and Serial RapidIO" on page 17 - Removed the statement "Note that core processor speed of 1500 MHz is only available for the PC8641D (dual core)" from Note 3 in Figure 22-1 on page 106 - Added Figure 17-2 on page 74 and notes - Added Note 8 to Figure 17-1 on page 73 and Figure 17-2 on page 74
0893A	04/2008	Initial revision.

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