TECH BRIEF

Teledyne e2v helps reduce power consumption in commercial processors

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ABSTRACT

System designers using commercial processors often wish to embed more processing capabilities in their application, while their authorized power budget may be limited by the project requirements & specifications.

In this paper, we will start by detailing some of the **constraints given to system designers in terms of power consumption** in commercial processors used in Aerospace & Defense (including, but not limited to Safety Critical Systems), then we will dive into the **different contributions of the total power consumption** of a device. We will finally explain in details where **Teledyne e2v is helping customers to reduce the power consumption on Microprocessors.**

We will illustrate the theory with a case study on how **Teledyne e2v was able to reduce**, on an Aerospace system, **the power consumption by 46% on an NXP T1042 Quad Core Power Architecture® Microprocessor** at 125C and in worst case conditions.

PROCESSING CAPABILITIES VERSUS POWER CONSUMPTION

There are multiple reasons to **embed more processing capabilities in a system:**

- Ability for the system to be **future proof**, i.e. still capable to work with the same expected behavior in 1, 5 or 10 years,
- Have **extra margin** for greedy applications, i.e. avoid a system freeze when newer applications are introduced,
- In addition, for **marketing purposes**...bigger is always better!

At Teledyne e2v, our Aerospace & Defense customers are also facing power budget constraints; those constraints are often linked with **Safety Critical** requirements.
Many parts of Avionics systems are indeed specifically designed to meet stringent requirements and withstand tough environments and extreme temperature conditions.

- Avionics electronics designers may have to create flight control systems, very similar to high performance computing servers, which **must fit in specific on board enclosures.** These systems, with or without added fans, have absolute maximum power dissipation constraints in order to **keep operating during extreme conditions.**

- System designers may also have to ensure **completely fanless designs** to improve their system's reliability. Designing a system without a fan allows production of less noise and enables operations at high altitude, even during loss of cabin pressure. This is often a critical requirement for sophisticated avionics systems or military weapon systems.
  Fans and other moving components increase chances of mechanical failure and lower Mean Time between Failure (MTBF).

- Avionics & space systems may also have **natural power consumption limitations** due to the embedded system itself.
  All of these requirements often link to constraints on power consumption of each part of the system, and in particular on the embedded Microprocessor, because it is one of the top components of the total system consumption.

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POWER CONSTRAINTS VERSUS COMPONENT SPECIFICATIONS

When diving into electronic specifications, such as on Figure 1 below, the power characteristics of a Microprocessor feature the core power dissipation under different modes, and depend on:

- Core frequency,
- Platform frequency,
- DDR frequency
- Junction temperature
- Power modes : Typical / Thermal / Maximum

Core frequency (MHz)	Platform/ FMan frequency (MHz)	DDR frequency (MHz)	V_{DD} (V)	SV_{DD} (V)	Junction temperature (°C)	Power mode	Power (W)		Total Core and platform power (W)[1]
							V_{DD}	SV_{DD}[8]	
1800	700/800	2100	1.0	1.0	65	Typical	8.5	0.9	9.4
					85	Thermal	11.4	0.9	12.3
						Maximum	14.3	0.9	15.2
					105	Thermal	14.4	0.9	15.3
						Maximum	17.3	0.9	18.2
1600	700/800	2100	1.0	1.0	65	Typical	7.7	0.9	8.7
					85	Thermal	10.7	0.9	11.6
						Maximum	13.2	0.9	14.2
					105	Thermal	13.7	0.9	14.6
						Maximum	16.3	0.9	17.2

Figure 1 : Extract of LS1046 power characteristics

Maximum power assumes in particular a Dhrystone running with activity factor at 100% (on all cores).
Thermal and maximum power are based on worst-case processed device.
Consequence: datasheets **naturally include some margin in the worst-case specifications** of the components.

This often translates into system designers and architects rejecting certain components, and selecting variants with lower performance, to **make sure that the maximum power fits theoretically** within the system constraints.
However, nothing shows that the maximum constraints will not be met in the actual system...but who is ready to take this risk?

On top of its extensive 35+ years' experience in manufacturing High Reliability processors, Teledyne e2v has developed a methodology **to offer to study specific power consumption requirements** from its customers, and deliver power-optimized parts when possible, i.e. **Microprocessor devices with even lower power consumption than was originally specified.**
This offer is well appreciated by customers since it **allows systems to embed more powerful and future proof components.**

Static & Dynamic power consumption

Well... as explained above, most component manufacturers are indicating, in their product specifications, maximum values; those values include margins that may cover process shifts, variations across time, maximum voltage and temperature conditions.

A final potential concern induced directly by this is that system designers may not be able to consider such large values.

Example:

- Can I afford 18.2 W power consumption at 105C for a Quad Core ARM® based Processor running at 1.8GHz if my power budget is 17.3W ?

- Should I instead clamp the Core frequency at 1.4GHz, i.e. reduce it by more than 22% to ensure the maximum budget is theoretically always met?

Going back to the basics of Microprocessor's power consumption, it is usually made up of **two contributions:**

- **Static Power consumption**
- **Dynamic power consumption**

Static power consumption variations

- Important variations from a device to device
  > We have observed, at Teledyne e2v, a **factor of 2 or 3** from one unit to another unit on a Quad Core Power Architecture Microprocessor

- Exponential increase with temperature (Figure 2)
  > Close to 0 (zero) watts at cold Temperature (-40C)
  > Can represent **up to 30 or 40% of the total device power consumption at 125C**

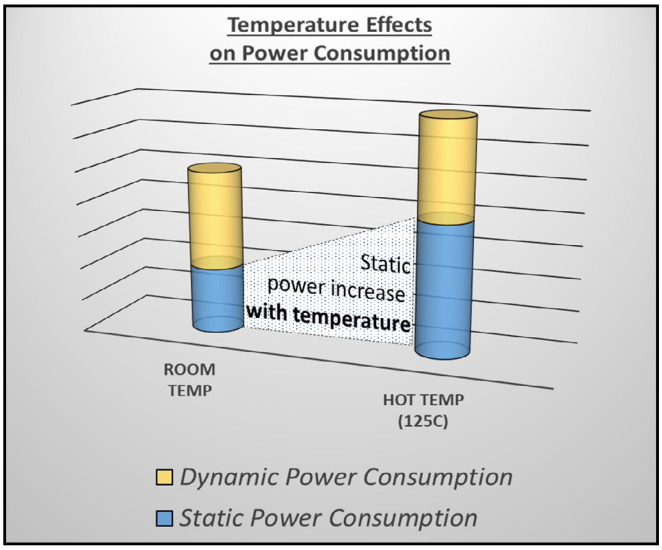

Figure 2 : Effect of Temperature on power consumption

Dynamic power consumption variations

- **Variations with frequency, number of cores running, processor load level**
- Low variations from one part to another
- Low variations from temperature

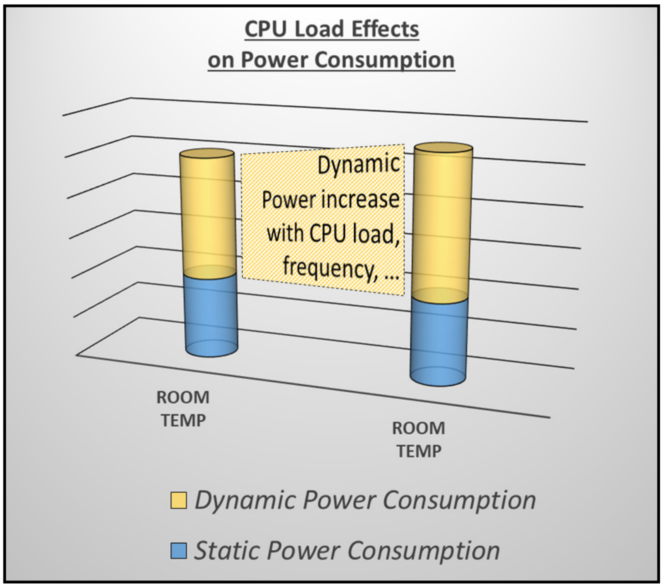

Figure 3 : Effect of CPU load on power consumption

The dynamic power consumption is 100% dependent on the customers' applications, and varies very little across temperature or between lots.

Consequently, by replicating the customer's biasing and application conditions, one can check and monitor the total power consumption on the customer's platform.
Well...up to now, ...this does not bring that much value, right, but consider the following, and how Teledyne is adding value on this.

Teledyne e2v added value on Power Consumption reduction

The value is optimized when one company has **access to the same tools, to the same test programs, test patterns, and to the same testers as the original manufacturer,** this starts to bring a lot of value ! **That company is Teledyne e2v.**

Teledyne e2v, with 35+ years of experience in selling processors to High Reliability markets, is providing this extra value to customers wishing to reduce the power consumption on their platforms.

Indeed, thanks to its **knowhow in uprating and up screening processors to High Reliability markets,** Teledyne e2v is also capable to replicate accurately the customers' use cases, biasing and application conditions, to work specifically on the static power consumption screening of the system.

Such activity can only be achieved when having :

- the **native test programs** from the original Microprocessor manufacturer,
  AND
- the **customer's use cases** as well.

As a result of Teledyne e2v's static power consumption study, Teledyne e2v is capable of selecting and **delivering microprocessor devices fitting within the maximum power constraints authorized by a customer project.**

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CASE STUDY: POWER CONSUMPTION REDUCTION ON T1042 QUAD POWER ARCHITECTURE CORE

In the following example, we describe how Teledyne e2v is successfully delivering T1042 Microprocessors (Quad Core Power Architecture) with a power consumption reduced by more than 45% versus the original specification.

Indeed, while the original specification indicates a power consumption of 8.3 Watts at 1.2GHz and 125C, Teledyne e2v is capable of delivering T1042 parts with a maximum power consumption of 4.5 Watts in the original customer's application, at 1.2GHz and 125C.

Below is a schematic representing the original constraints from the customer, versus the specification of the product at 1.2GHz and 125C.

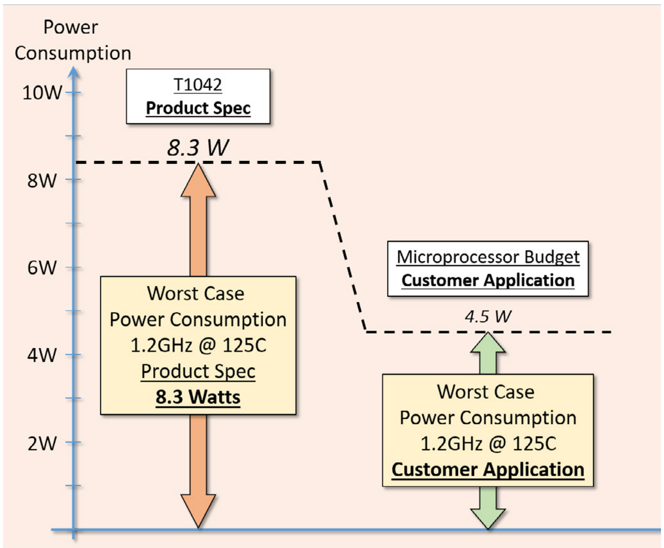

Figure 4 : Specification versus customer power budget

Figure 4 shows that nothing allows the customer to think that a T1042 device, running at 1.2GHz, will be able to consume less than 4.5 Watts at 125C. And by far!

What would be required to accomplish this is a deep analysis of the power contributions, to better understand the **split between static & dynamic power**, and make sure that the devices planned to be used in the application fit with the maximum power budget.

On one hand, a check of the static & dynamic consumption is technically feasible. However the distribution of the components delivered by the manufacturer does not prevent some spread in the parts delivered, therefore nothing can be concluded from this technical check.

Thanks to the original NXP test programs and the knowledge and capability to tune them, **Teledyne e2v is able to perform a technical analysis on the power consumption of T1042 devices.**

Teledyne e2v has highlighted the following split between static and dynamic power consumption at 125C, and 1.2GHz clock frequency, see Figure 5.

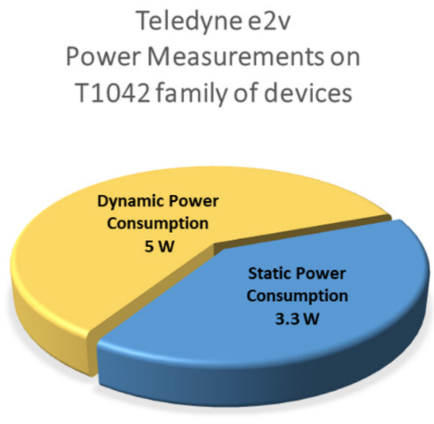

Figure 5 : T1042 power measurements at 125C

Moreover, Teledyne e2v has led technical discussions with the customer allowing the companies to nail down a maximum dynamic power consumption of 2.5 Watts on the customer application, at 1.2GHz clock frequency and 125C.

This results in a maximum of 2 Watts allowed for the static power consumption of the required T1042 Microprocessor devices.

Another differentiator is highlighted here: **Teledyne e2v's capability to sort, screen and deliver parts which fit its customers' requirements.**

In practice, the results of the collaboration are represented below on Figure 6.

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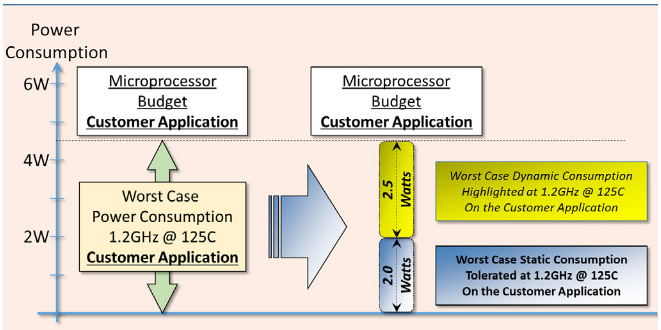

Figure 6 : Split between power contributions in the customer application

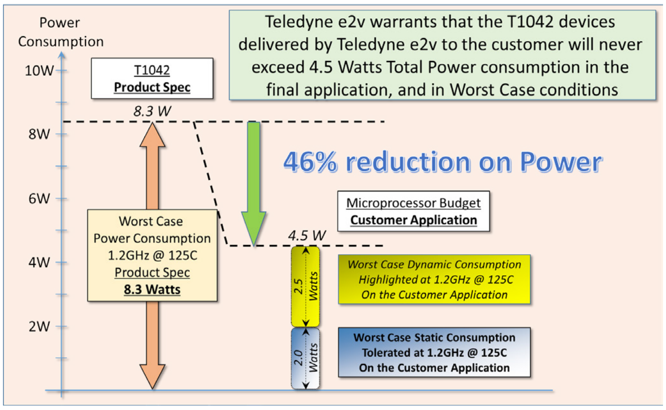

Figure 7 : Power consumption total reduction

Finally, Figure 7 highlights how Teledyne e2v is capable of delivering T1042 screened units, qualified up to 125C, and guaranteed to have a global power consumption below 4.5 Watts at 125C and 1.2GHz clock frequency.

The conclusion of this case study is that **Teledyne e2v is capable of delivering T1042 with 46% power consumption reduction,** versus what one would expect by reading the T1042 specification.

Multiple environments and projects should find interest is such power reduction capabilities beyond Space, Aerospace & Defense and Teledyne e2v is ready to study each customer's specific request.

LEARN MORE:

PRODUCTS:

- Teledyne e2v T1042 Hi-Rel Datasheet
- Teledyne e2v Hi-Rel Processors
- Qormino packaged processing solutions

PRESS RELEASE:

- BAE Systems' mission computer press release
- First military qualified Arm® based processor press release

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