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Implementing the EV12AS200

Application Note

Introduction

This application note aims at providing some recommendations to implement the EV12AS200 12-bit 1.5 Gsps single core ADC in your system.

It first presents the ADC input/output interfaces and then provides some recommendations as regards the device settings and board layout to obtain the best performance of the device.

This document applies to the:
• EV12AS200 12-bit 1.5 Gsps ADC
This document should be read with all other applicable documentation related to this part, (datasheet, errata sheet ,….).

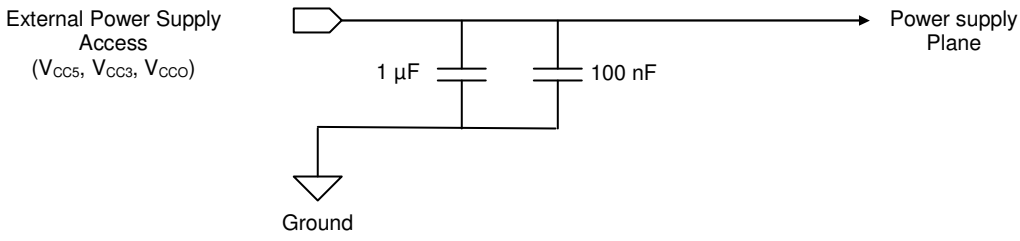
For further information and assistance please contact **Hotline-bdc@e2v.com**

1.1 BYPASSING, DECOUPLING AND GROUNDING

All power supplies have to be decoupled to ground as close as possible to the signal accesses to the board by 1 µF in parallel to 100 nF.

Each incoming power supply is bypassed at the banana jack by a 1 µF Tantalum capacitor in parallel with a 100 nF chip capacitor. Each power supply is decoupled as close as possible to the EV12AS200ZPY device by 10 nF in parallel with 100 pF surface mount chip capacitors.
Note: The decoupling capacitors are superimposed with the 100 pF capacitor mounted first.

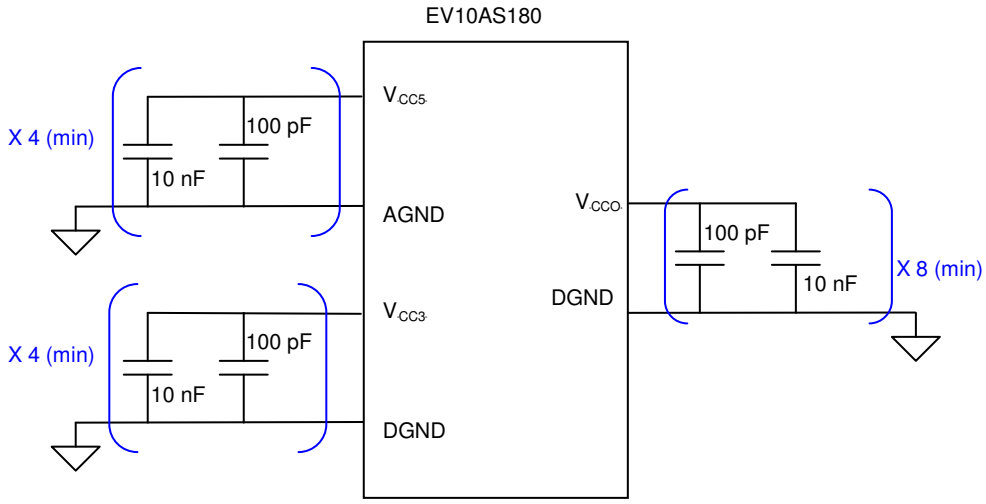
Figure 1 EV10AS200 Power supplies Decoupling and grounding Scheme



Each group of neighboring power supply pins attributed to the same value should be bypassed with at least one pair of 100 pF in parallel to 10 nF capacitors. These capacitors should be placed as close as possible to the power supply package pins.
The minimum required number of pairs of capacitors by power supply type is:

4 for V_{CC5}
4 for V_{CC3}
8 for V_{CCO}

Figure 2 EV10AS200 Power Supplies Bypassing Scheme



Each power supply has to be bypassed as close as possible to its source or access by 100 nF in parallel to 1µF capacitors.

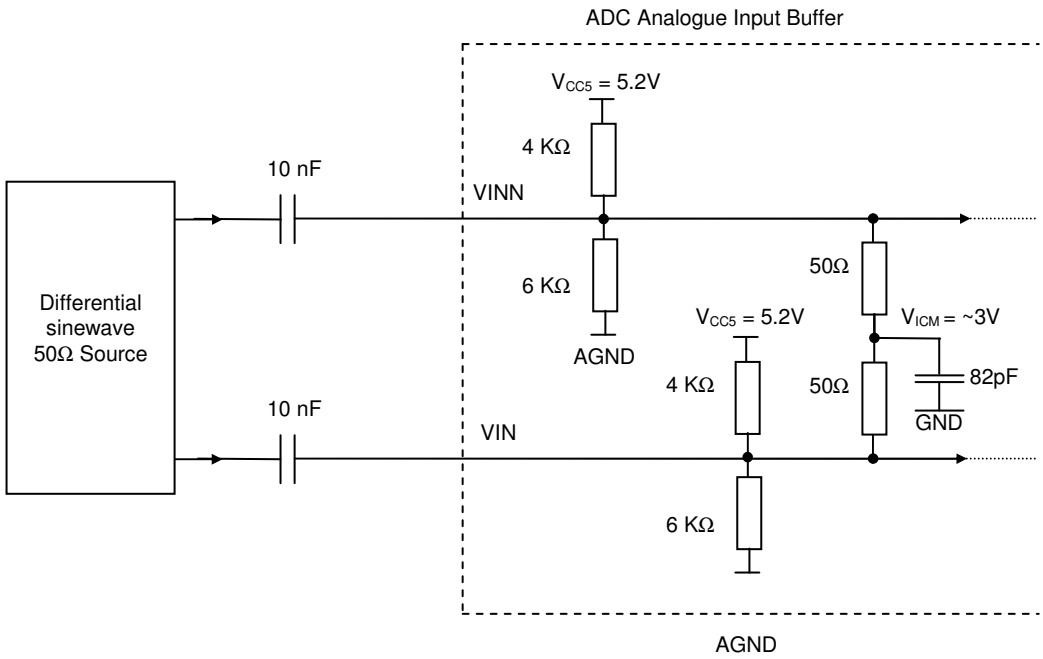
1.2 ANALOGUE INPUTS (VIN/VINN)

The analogue input should be used in differential mode. If a single-ended source is used, then a balun (transformer) should be implemented to convert the signal to a differential signal at the input of the ADC.

1.2.1 Differential analog input

The analogue input should be AC coupled as described in Figure 3.

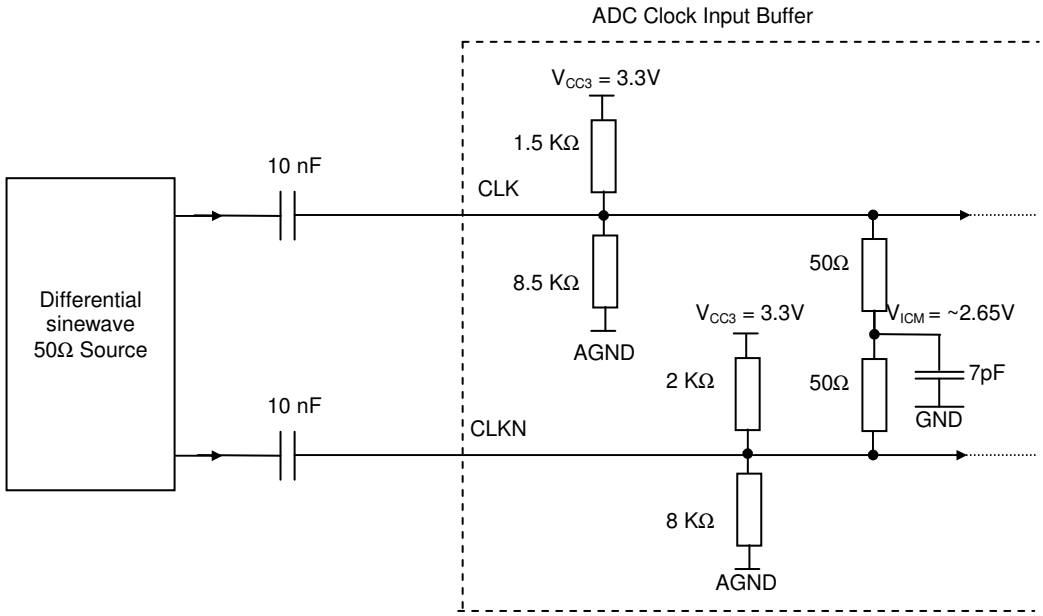
Figure 3 Differential analogue input implementation (AC coupled)



1.3 CLOCK INPUTS (CLK/CLKN)

Differential mode is the recommended input scheme. Single-ended clock input is not recommended due to performance limitations. If a single-ended source is used, then a balun (transformer) should be implemented to convert the signal to a differential signal at the input of the ADC.
Since the clock input common mode is 2.7V, we recommend to AC couple the input clock as described in Figure 4.

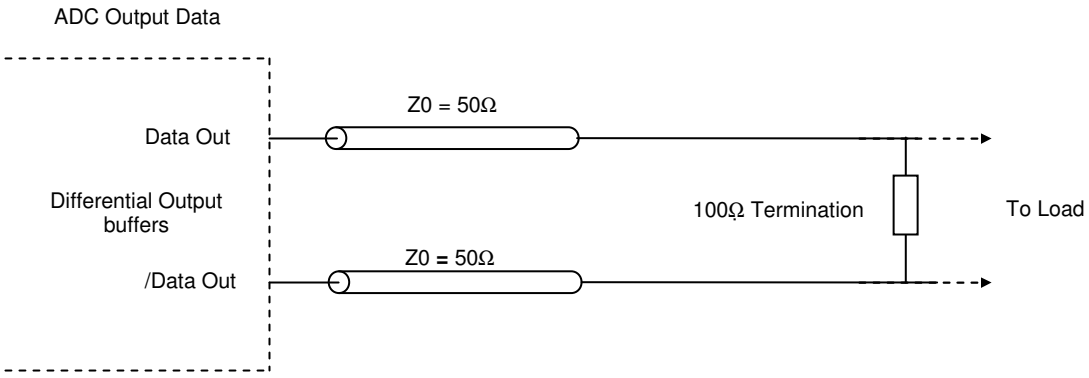
Figure 4 Differential clock input implementation (AC coupled)



1.4 DIGITAL OUTPUTS

The digital outputs are LVDS compatible. They have to be 100Ω differentially terminated.

Figure 5 Differential digital outputs Terminations (100Ω LVDS)



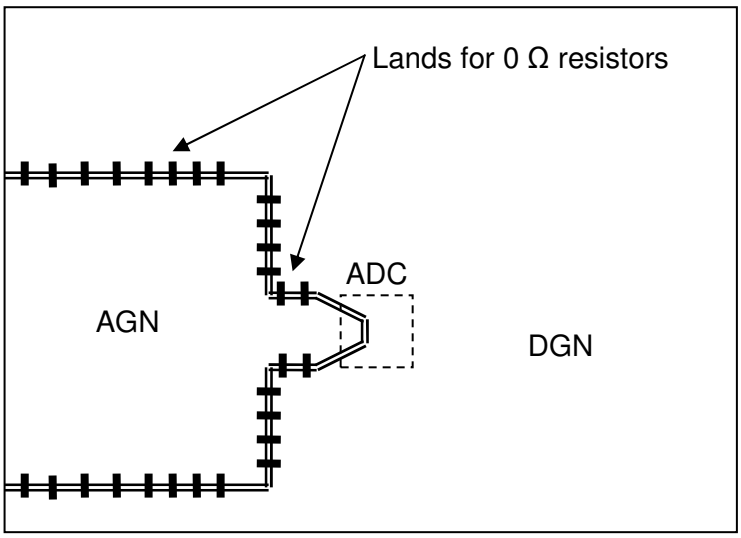
If the ADC is used in 1:1 or 1:2 DMUX modes, the unused ports can be left open (no external termination required).

PCB Layout

Ground Layers

It is recommended to have 2 planes for the AGND and the DGND on the PCB. These planes can be reunited via 0 Ω resistors (28 locations for 0 Ω resistors are recommended). Only the input clock and analogue input are referenced to AGND, the other parts of the ADC are referenced to DGND.
Important note: AGND and VCCO should not be superimposed in order to avoid coupling effects. VCC3 and VCC5 are referenced to AGND while VCCO is referenced to DGND.

Figure 6 AGND and DGND planes (bottom layer)



However for complex designs using more than one converter it is recommended to use a single ground plane and to ensure with good component placement that analog and digital sections are separated.as shown below.

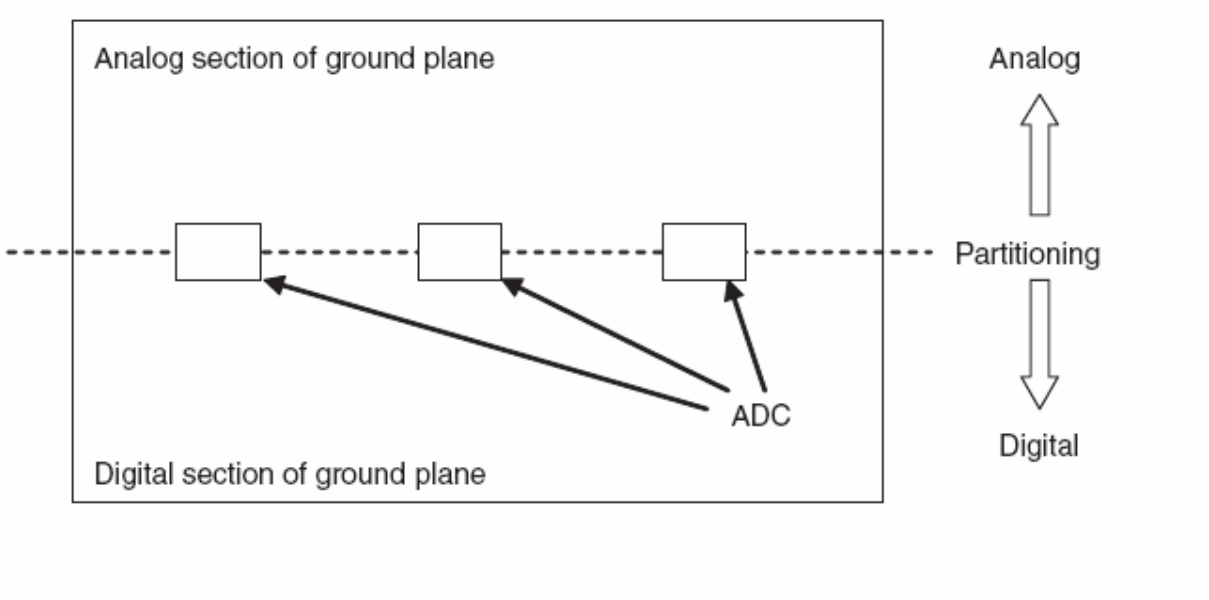


Figure 7 Multi-converter ground plane

For further details see applications note 0999B_Design Considerations for Mixed Signal PCB Layout.

Layer stack-up

An ideal stack-up will be a ground plane under each other plane (signal or power). In this case, a signal should not be disrupted by the return current of another signal.

If it is not possible for cost reasons, place each signal layer in between the ground plane and power (or ground) plane. Inductance is directly proportional to the distance an electric charge has to cover from the source of an electric charge to the ground. As the distance gets shorter, the inductance becomes smaller.

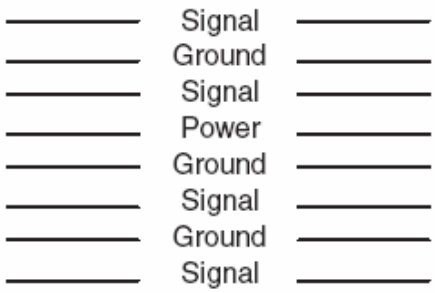


Figure 8 **Ideal Layer Stack**

Recommended Supply Regulators

It is recommended to use low noise LDO style regulators for the Vcc5 analog supply voltage.
A recommended device is the LT1963.

PCB Traces

Analogue Inputs/Clock Input

The following dimensions are recommended.

50Ω lines matched to ± 0.1 mm (in length) between VIN and VINN or CLK and CLKN.

1270 µm between two differential pairs. 400 µm line width.

40 µm thickness.

870 µm diameter hole in the ground layer below the VIN and VINN or CLK and CLKN ball footprints.

AC signals traces = 50Ω microstrip lines DC signals traces
In addition, the lines for VIN, VINN and CLK, CLKN are matched to one another within ±1mm.

A clearance in the ground plane below the CLK, CLKN and VIN, VINN package lands is necessary.
Note: These values have been calculated with RO4003 dielectric material.

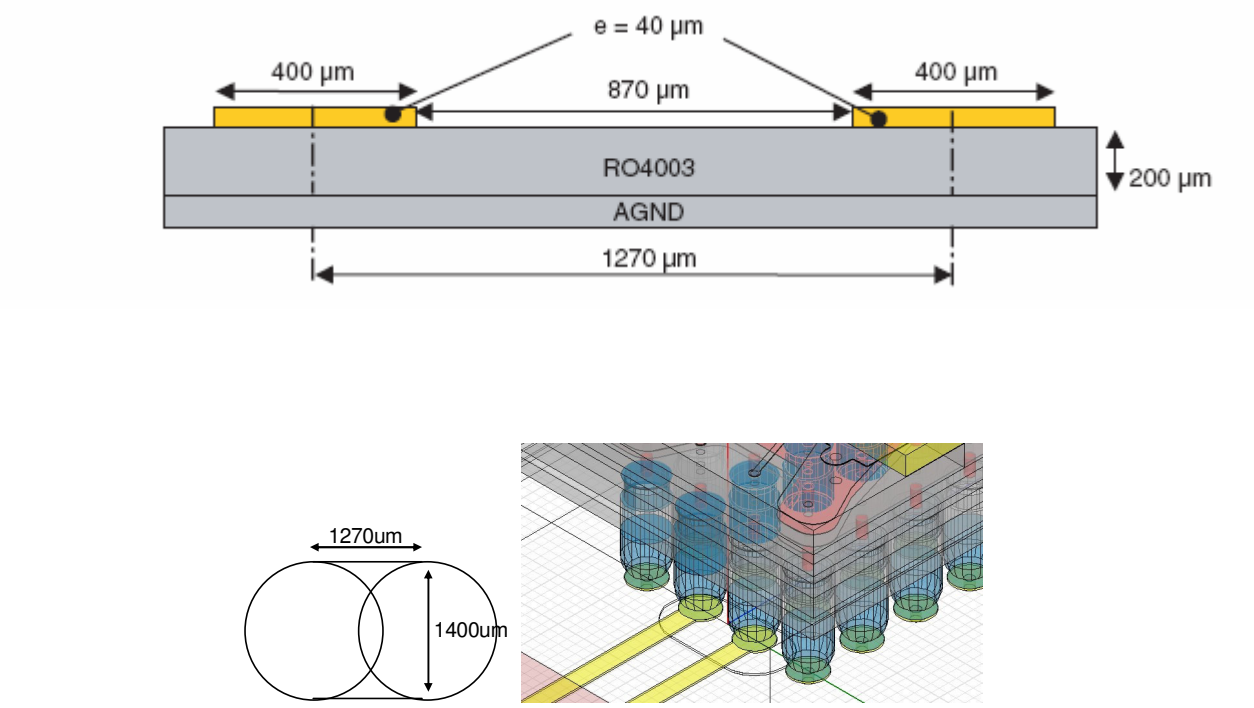


Figure 9 **Analog and Clock Inputs**

SYNC, SYNCN A power up reset ensures that the first digitized data corresponds to the first acquisition. An external differential LVDS Reset (SYNC, SYNCN) can also be used. RES function allows changing the active edge of the RESET signal.

50Ω lines matched to ± 0.1 mm (in length) between SYNCP and SYNCN
1270 µm between two differential pairs
400 µm line width
40 µm thickness
870 µm diameter hole in the ground layer below SYNC, SYNCN ball footprints

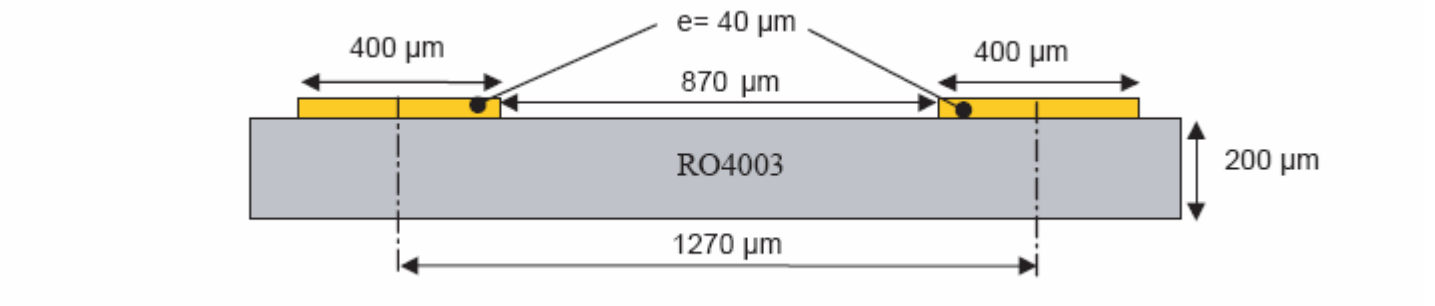


Figure 10 **SYNC Inputs**

Digital Output Data

The high speed differential output signals (digital output, data ready output), should be routed in parallel with 50 ohm impedance, 370 µm width and a pitch of 0.77 mm.
Max difference between any two signals = ±1.5mm. (implying +/- ~12ps skew)
Max difference between longest and shortest data per port = ±1mm.
Max difference between two signals of the same differential pair (Xi, XiN) = ±0.5mm (where X = A and B, i = 0…9). Note: These values have been calculated with RO4003 dielectric material.

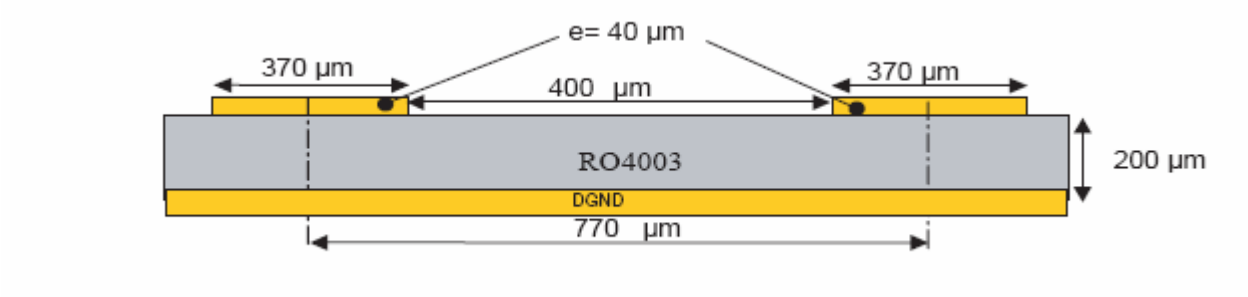


Figure 11 **Digital Data layout**

RS, TM, SDA, SDAEN, GA, OA, SA, RESETN, MODE_n, Diode and CMIRef These are "static" signals. They are routed in single-ended 50 ohm impedance. ***Figure 2-4.*** Recommended Routing on RO4003 for static Signal

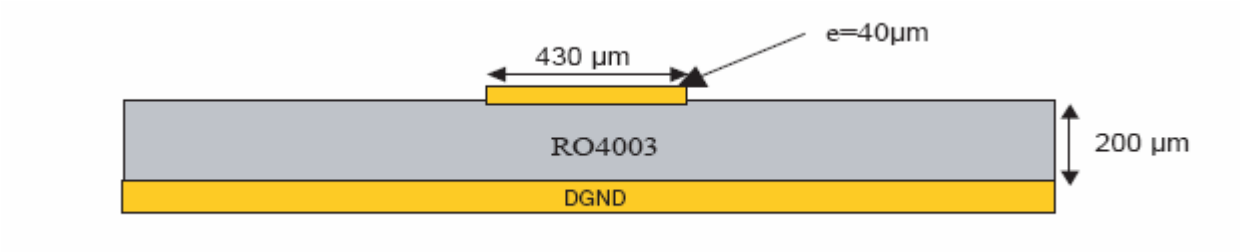


Figure 12 **Single Ended Inputs**

Choice of oscillator

For a 12 bit ADC running at such high sampling rates, clock jitter becomes a critical parameter.
The effect of the clock jitter on the sampled signal noise floor can be calculated using the phase noise figures given by the PLL manufacturer.
In fact for large bandwidth converters the phase noise close to the carrier is not the dominant source and the integral of the phase noise floor becomes more important.

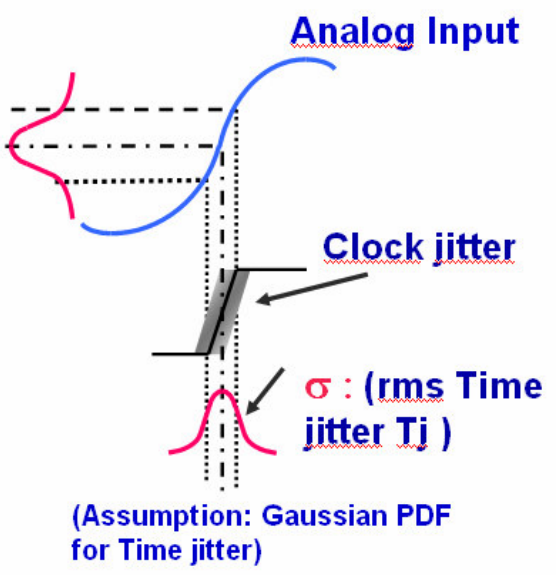


Figure 13 **Effect of Jitter on Signal**

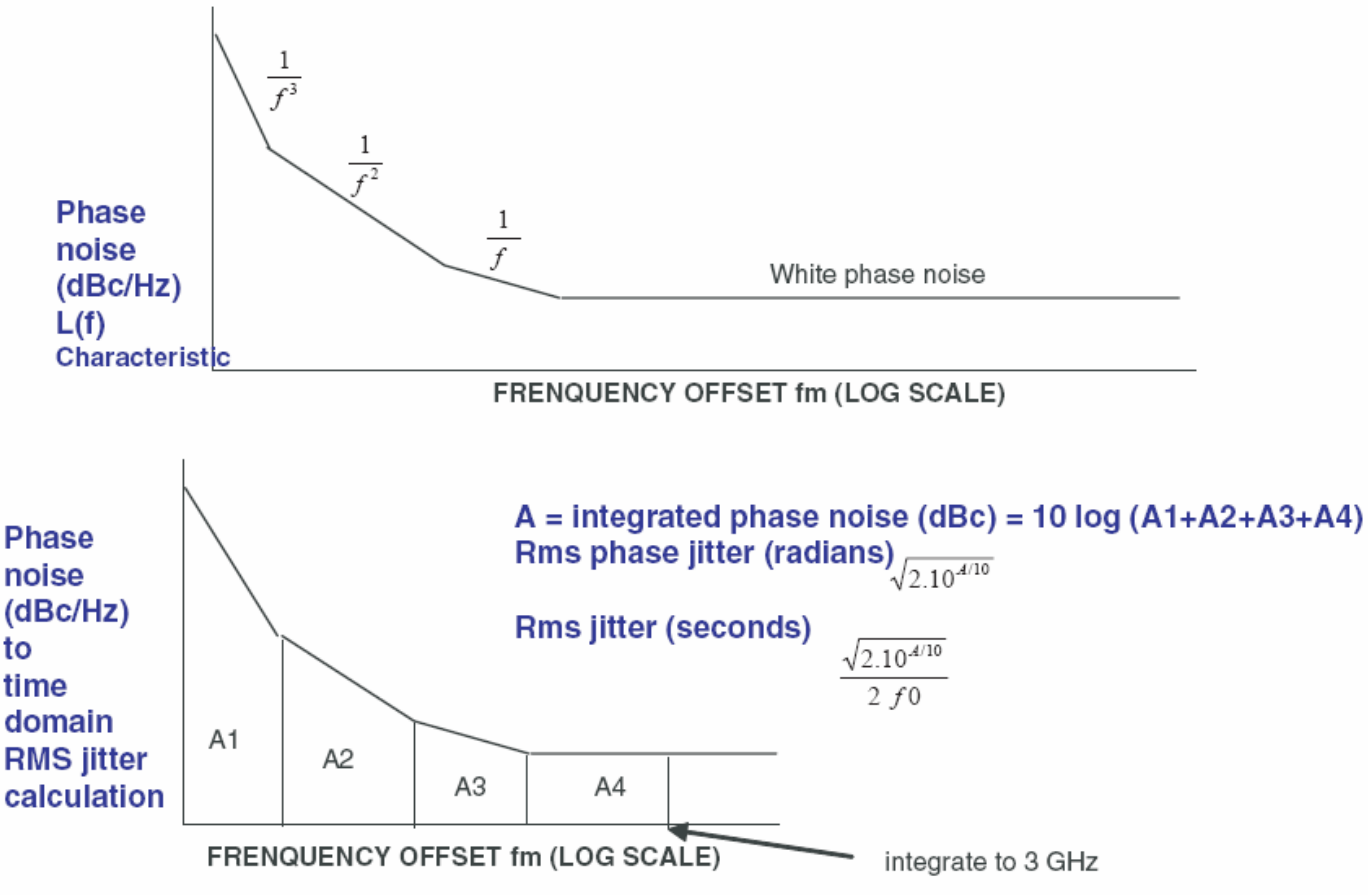


Figure 14 **Jitter Calculation from Phase Noise**

Given the recommendation for 100 fs maximum clock jitter to achieve optimum performance; a PLL with phase noise floor approaching 155 dBc /Hz (at 10 MHz of carrier) should be considered.

Example

Agilent Clock source phase noise : - 155 dBc/Hz ; 5.5 GHz BW

Phase Noise Spectral density (10log(Rad2/Hz) expressed in dBc/Hz : - 155 dBc/Hz (Agilent)

Integration Bandwidth assumption (clock buffer input BW) : 1 MHz up to 5.5 GHz = ~ 5.5 GHz :

Integrated phase noise in dBc : - 155 dBc + 10log(5.5E09 - 1.E06) = ~ -155 + 97.4 = - 57.59 dBc

Integrated Phase noise in radians (rms) : $\sqrt{2.10^{A/10}}$ = $\sqrt{2.10^{-57,6/10}}$ = 1,86.10-3 radians (rms)

➔ Arms = 1.86.10-3 radians (rms) / SQRT(Hz)

➔RMS Time Jitter (seconds) for a 3 GHz Carrier fc: = $\frac{\sqrt{2.10^{\frac{A}{10}}}}{2.\pi.fc}$ = $\frac{\sqrt{2.10^{\frac{-57.6}{10}}}}{2.\pi.3.10^{9}}$ $\frac{1,86.10^{-3}}{2.\pi.3.10^{9}}$

➔ Clock source Jitter (Agilent) = 98 fs rms

Recommended Clock source manufacturers are Crystek, Peregrine and Linear Technology

Improving SFDR using a LUT

The plot of the INL shows an S shape. This causes a high third harmonic at larger input signal amplitudes.

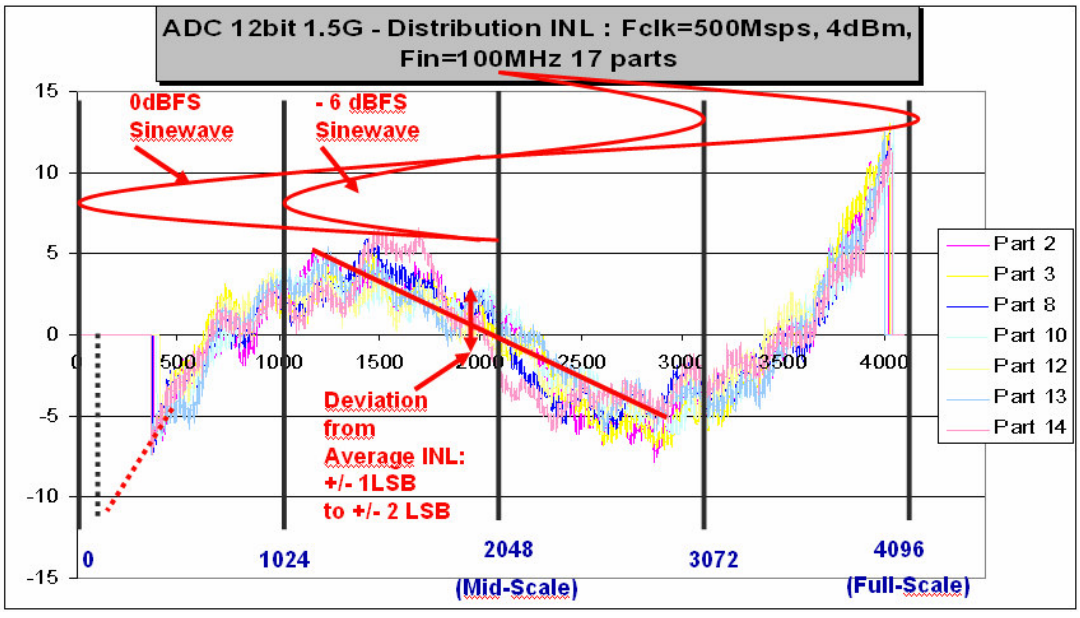


Figure 15 **INL Curve**

The figure above shows that a large amplitude signal will see large variation in INL which will cause non-linearity of response and hence higher harmonics; whereas the smaller signals are mainly in a linear part of the INL curve.

The INL shape has been measured over multiple parts and over temperature and supply and has been seen to be stable. This gives the possibility to calibrate for the INL in a post processing stage.

This calibration stage simply adds or subtracts a the relevant number of LSBs given by the INL calibration shape for the amplitude of the sampled signal.

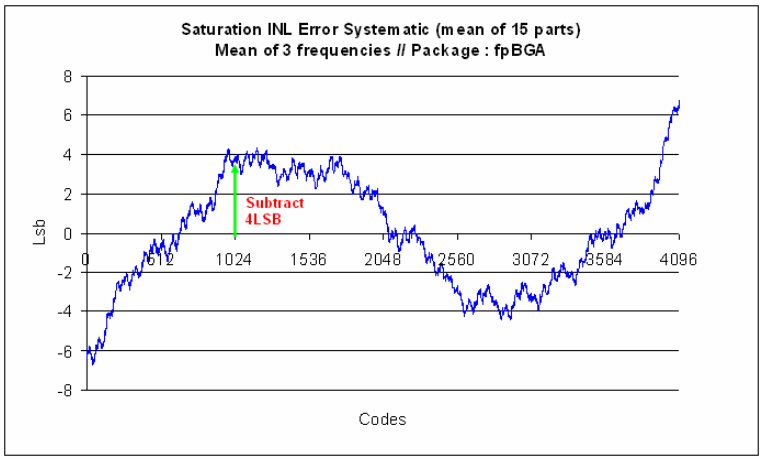


Figure 16 INL Calibration

The image below shows the improvement gained in SFDR by using this calibration look up table.

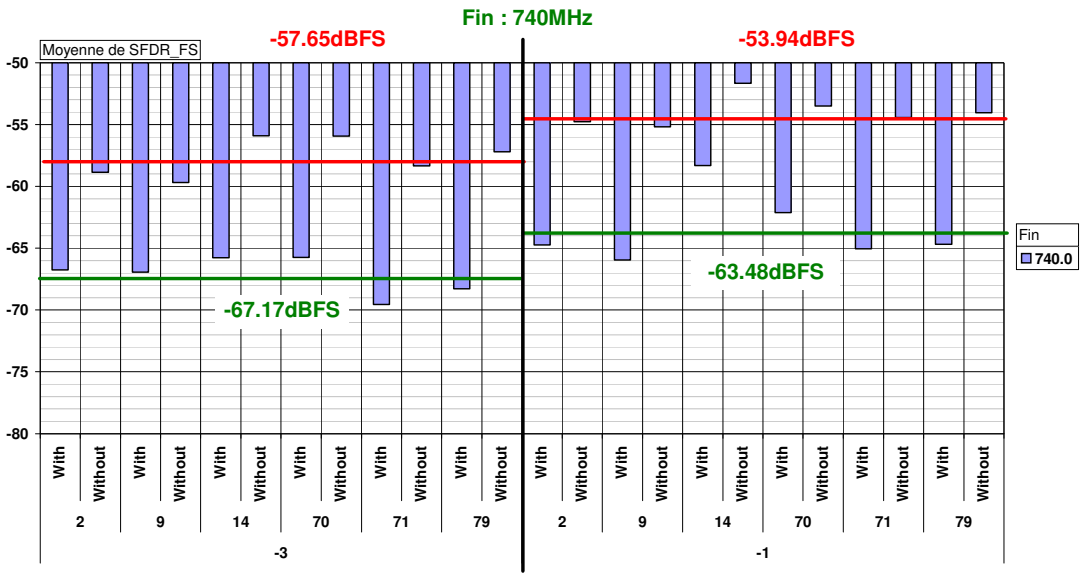


Figure 17 Look Up Table improvement on SFDR.

Trig signal

The Trig signal can be used to synchronize the data with an external event or signal captured by a comparator. This function is selectable using the 3WSI.
A logic signal input to the SYNC pin will be output on the PCB pin in synchronisation with the data that was at the input of the ADC at the same time.

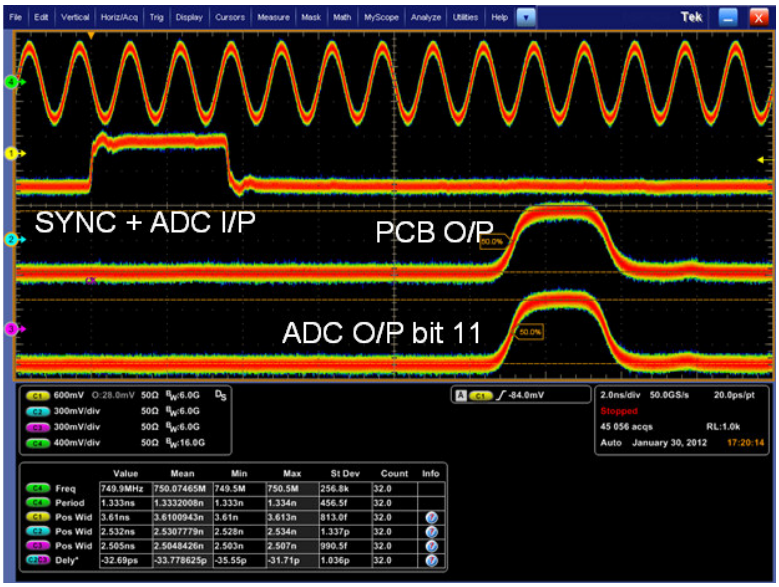


Figure 18 **Trigger Signal**

The image shows a signal input to SYNC and the ADC input simultaneously. The signal appears at the output at the same time?.

SYNC min Pulse

The minimum pulse width for the SYNC to reset the control circuits is 1 period of the ADC clock.

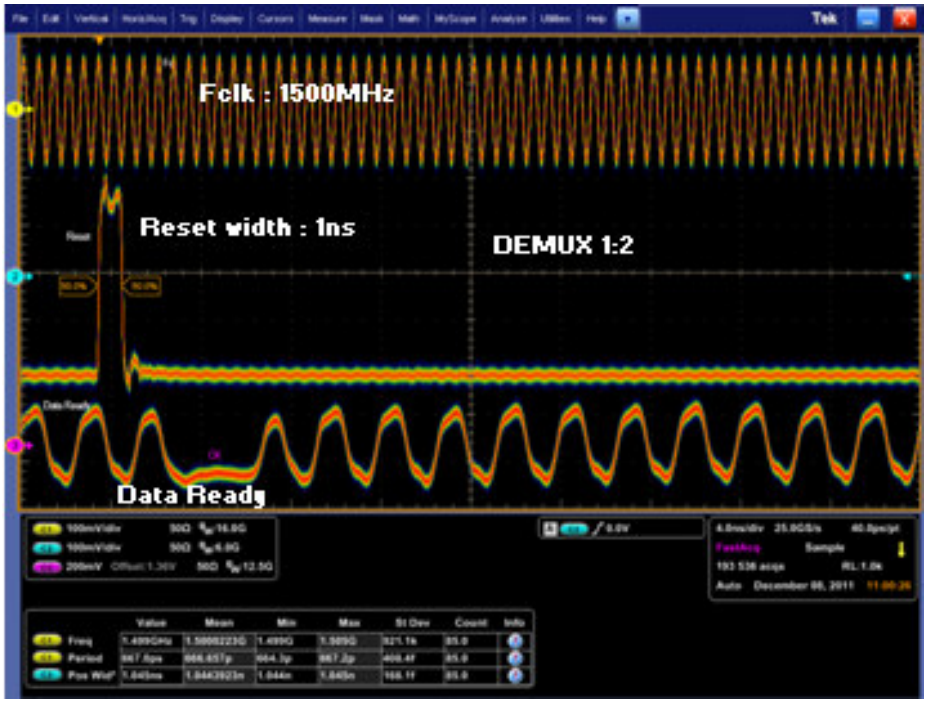


Figure 19 **SYNC Pulse operation**

SDA (Sampling Delay Adjust)

The use of this function reduces slightly the performance of the part. A 1dB reduction in SNR can be seen when this function is activated. In addition the coarse SDA can reduce further the SNR depending on the step. The scale is approximately 0.2dB per step, so at SDA coarse = 0 there is no loss in performance.
The fine SDA adjust reduces the SNR by 0.2dB no matter what step value is used.

Offset

An offset code of 2048 will give a nominal offset. Reducing this value will increase the offset, increasing the register value will reduce the offset.

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