WHITE PAPER

Advanced wide band sampling solution for direct digitization of the K-band – extending the boundaries of RF possibility.

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TELEDYNE e2v
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INTRODUCTION

In a world of exploding digital content, growing numbers of Internet users and connected IoT devices, there's an insatiable need for ever expanding communication network capacity. To that end, Teledyne e2v, in its ongoing push to explore the boundaries of digital microwave sampling has recently demonstrated an experimental set-up. It provides direct digital down conversion from the K-band . This continues work previously introduced at the **ESA MTT workshop** earlier this year that proposed direct digital K-band frequency synthesis using the **EV12DS480** broadband DAC; work that was further documented in **a technical paper[1] and recent webinar[2].**

PROJECT OBJECTIVES

This project aims to build a 24 GHz analog front end able to directly digitise signal energy in the microwave K-band (i.e. in the range of frequencies from 18 to 27 GHz). A target spurious free dynamic range (SFDR) of better than 50 dBc was to drive our experimental philosophy.

The microwave front-end board (FEB) developed associates two pre-existing gigahertz fast components developed by separate Teledyne entities (Teledyne Scientific and Teledyne e2v). Lab testing was performed on the high-performance FEB combining the EV12AQ600, a 12-bit broadband data converter with the **RTH120,** an ultra-high frequency, dual circuit track-and-hold amplifier (THA).

The former, capable of sampling at up to 6.4 Gsps, has a full power input signal bandwidth of 6.5 GHz. The track and hold is billed as having excellent linearity and a bandwidth stretching all the way out to 24 GHz. Thus, by applying Nyquist folding principles and suitable sampling frequency selection, it should be possible to down convert directly from the K-band into the baseband, using the ADC to acquire useful signals without additional down conversion circuitry. The guiding principle for this effort is the idea of versatile software defined microwave reception bringing increased agility to RF design whilst at the same time simplifying RF signal acquisition system design and potentially lowering power. Also, at the back of our minds in developing this project is the hope to gain realized system power savings in future.

Key parameters of active devices

EV12AQ600 ADC

- Quad core ADC supports 1, 2 or 4 channel operation
- Sample up to 6.4 GSps in fully interleaved mode
- 6.5 GHz input bandwidth (-3dB)
- Integrated broadband cross point switch
- Sync chain feature for multi-channel synchronization

RTH120 THA

- 24 GHz input bandwidth
- Dual THA enables output hold for more than half clock cycle
- Full differential design

This article documents the state of this research, expands on the current findings and highlights some of the improvements yet to be made.

The objective of the series of planned tests was to determine the effective limits of direct down conversion in the K band (18 to 27 GHz) of current technology. Three specific problems were identified from initial spurious free dynamic range testing as follows:

- the effect of input signal power on THA performance
- the impact of low frequency calibration on the ADC 's interleaving performance when working in high Nyquist zones
- the impact of integral non-linearity (INL) errors within the ADC again when sampling in high Nyquist zones

Ultimately, Teledyne e2v hopes that the learnings from this project leads towards a next generation integrated product design capable of working within the K-band.

A ROCKY PROJECT START

The basic block diagram for the front-end board (FEB) set-up is shown in figure 1. The FEB was designed to accommodate both the broadband ADC and the THA acting as the input stage to the ADC. Looking closer at the FEB figure 2, it contains some additional support components including: a power splitter, a phase shifter and baluns. The board also provisions two separate inputs; one bypassing the RTH120 for optimized performance up to 6 GHz for first and second Nyquist zones sampling (not shown here), a second for broadband operation from 6 to 24 GHz. At the start of this project, the RTH120 was a pre-production part undergoing optimization efforts.

The initial configuration of this experimental system assumed the following ADC default settings:

- Input bandwidth (6.5 GHz)
- 1-channel mode, all four cores interleaved for maximum sample rate (e.g. 6.4 GSps)
- The sample frequency was set to 5 GSps
- Interleaving calibration was set per the standard default datasheet settings, referred to throughout this discussion as CalSet0

Figure 2 - Photo of initial prototype FEB on its carrier board

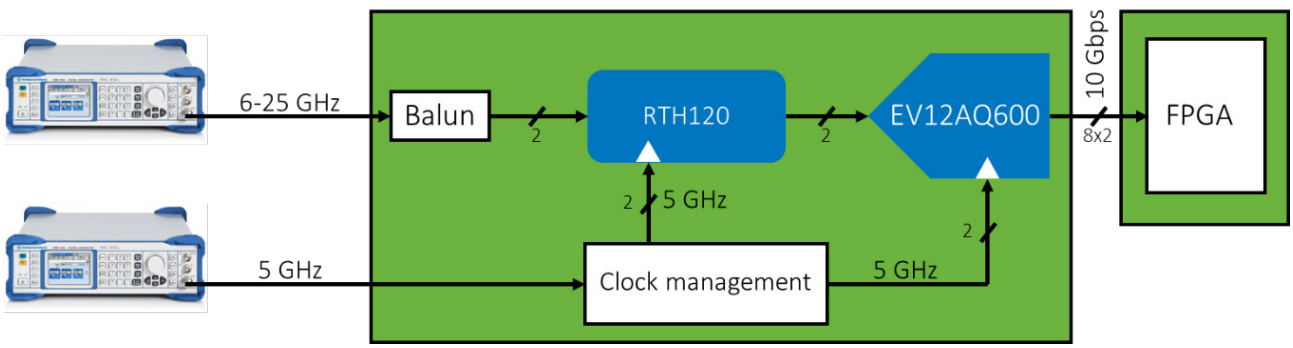

Figure 1 - FEB test evaluation set up showing key active devices

CURIOSITY SURROUNDS THE FIRST SET OF DYNAMIC TEST RESULTS

Initial measurements performed with the FEB showed variability in the spurious free dynamic range (SFDR) response (figure 3). Two separate sweeps were performed at different signal full-scale ranges (SFSR) of the ADC. This sweep covered signal frequencies out to in excess of 30 GHz. The graph on figure 3 shows a zoom on the 17 GHz to 25 GHz range.

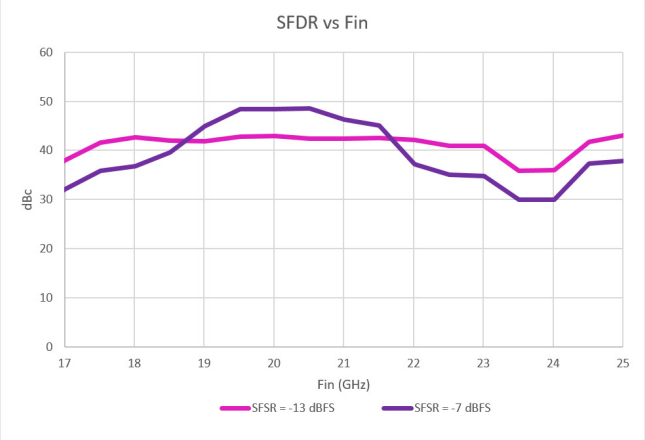

Figure 3 - The baseline FEB performance (SFDR swept from 17 to 25 GHz)

INSPECTING INITIAL RESULTS

Clearly the SFDR characteristic provides some diagnostic value, giving insight to determining where to hunt for future dynamic improvements. Thoughts arising from considering these results (per figure 3) include the following observations:

- Lower input signal power leads to better SFDR flatness (compare -7 with -13 dBFS – figure 3)
- Initial experimental set-up unlikely to reach our 50 dBc SFDR goal

The first step towards improving performance is to properly identify which signal spurs are limiting the SFDR. The following plot (figure 4) maps the main spurs expressed in dBFS for input levels of -7 and -13 dBFS.

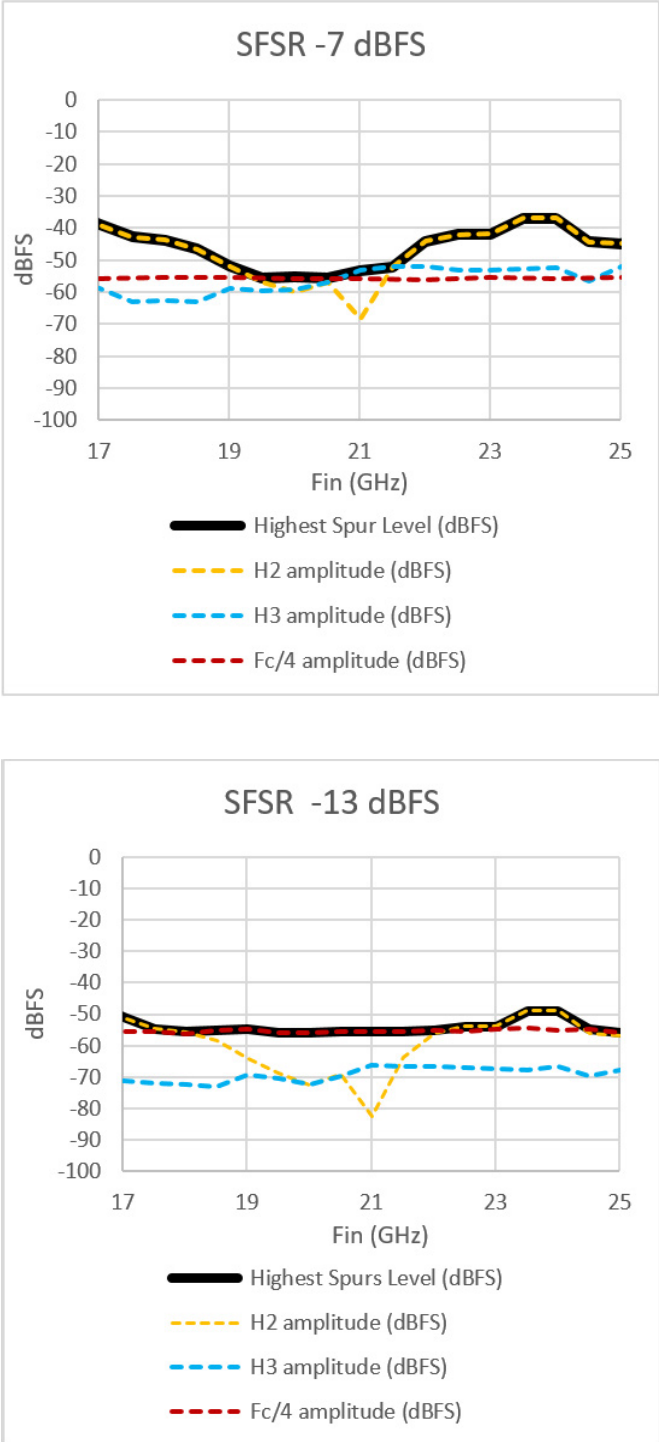

Figure 4 - The baseline FEB performance at two signal powers (SFDR swept from 17 to 25 GHz)

From these plots, depending on the frequency range and input level amplitude, various spurious frequency components are to be seen as the source of the SFDR variations mapped by the aggregate highest spur level trace. These plots highlight the impact of second (H2) and third harmonic (H3) as well as contributions from the sample clock (Fc/4). Continuing this visual assessment, the following are observable:

- Most noticeable from the highest spur level (dark trace) is the dominant impact of H2 especially at -7 dBFS.
- If H2 could be improved, then the next most impactful effect is clearly Fc/4 performance, which dominates the reduced signal level plot (- 13 dBFS). However, at both signal power levels shown, Fc/4 limits SFDR to approximately 58 dBFS (between 18 GHz and 22 GHz). Without addressing this factor it will be hard to yield further dynamic improvement. An Fc/4 problem suggests some issues resulting within the compounded interleaved cores of the ADC. The source of spurious signals is the offset mismatch.
- These plots suggest an optimized solution might yield SFDR of between 50 to 60 dBc at -13 dBFS.

In hunting for dynamic improvements, the only way to improve the performance of the THA (by reducing its H2) according to the product data is to reduce input signal level. It can then be useful where the SFDR is limited by the H2, below 19.5 GHz above 21.5 GHz for example with a SFSR of -7 dBFS.

OPTIMIZING DATA CONVERTOR PERFORMANCE

On the other hand, the ADC offers more degrees of freedom beyond its default operating point. Initial testing highlighted some clear issues with the precision of core interleaving. This should not be a surprise. The standard interleaving calibration (ILG) is established in the factory during production testing. Obviously, it is optimized for baseband operation, not for the high bandwidth application this research aspires to.

A detailed review of ADC interleaving established that the biggest source of spurs was from offset mismatches. The offset impact across a range of frequencies was measured and through a tweaking process it became apparent that there were large improvements possible with Fc/4 spur reduction (figure 5). With a focus on K-band operation, a calibration performed at 21.5 GHz gave particularly encouraging results.

The K-band performance of the system with pre- and post-interleaving calibration is shown in figure 5. The upper curve shows the default setting (CalSet0) and the lower curve, the result of improved high frequency calibration. In the latter case, offset, gain and phase mismatches are compensated. This is a significant improvement as the system gains almost 15 dB SFDR enhancement across the whole K-band.

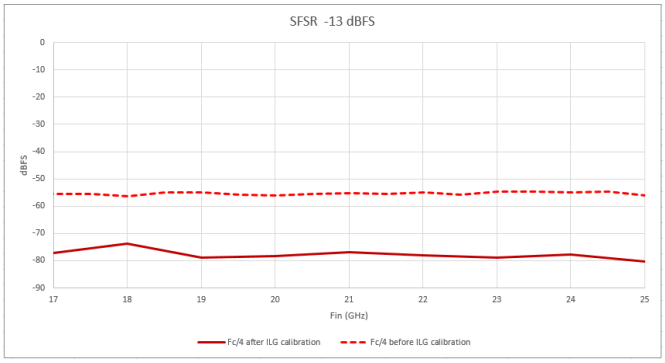

Figure 5 - Impact of calibrating ILG

MOVING BEYOND INTERLEAVING CALIBRATION

For some frequencies, H2 was lower and H3 becomes dominant as seen in both plots around 21 GHz (figure 4). In this case, we have another potential lever to try to reduce spurious contributions offered by the ADC: the calibration for INL.

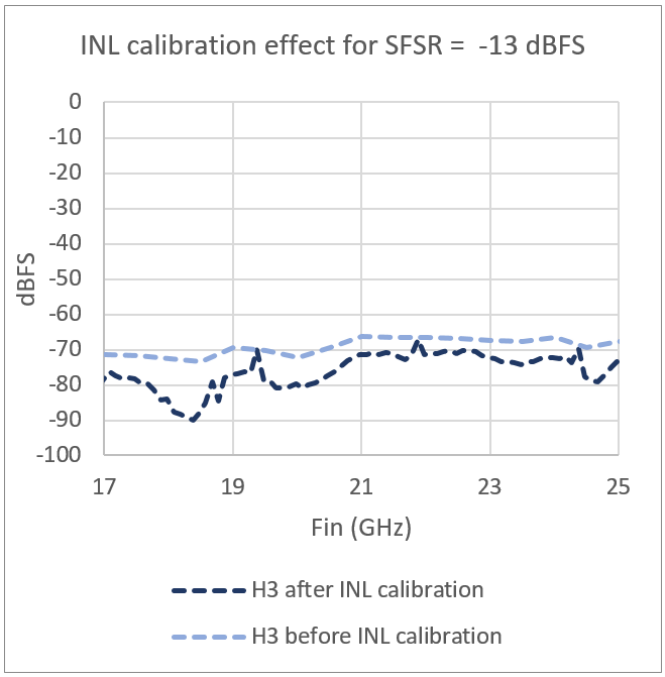

Figure 6 - Impact on H3 with INL calibration

Though options to improve performance further seem limited, the integral non-linearity performance of the convertor (INL) can impact H3. And, just as with interleaving (ILG), INL calibration is normally optimized for baseband operation in production test. However, Teledyne test engineers felt there would be some additional dynamic improvements yielded if INL was specifically re-calibrated for operation in the higher Nyquist zones.

INL adjustment is not a user programmable feature, nor should it be. It proves challenging to adjust in a meaningful way. In principle, to improve INL excursions from the ideal transfer function are compressed as much as is viable. Some engineering work was needed to establish a test rig to allow for the adjustments required.

Having minimized high frequency INL as much as possible, it was established we could benefit from between 3 to 5 dB improvement in H3 over the 17 to 25 GHz range (figure 6).

What is INL? For an ADC, INL quantifies the maximum departure from the idealized straight-line transfer function of the device. In precision electronics, INL is to be expected to be better than 0.5 LSB over the full-scale range of the convertor. Realistically that is not possible in broadband interleaved systems. In the case of the EV12AQ600 operating in fully interleaved mode INL, is specified at fin = 100MHz as +/- 4.5 LSB.

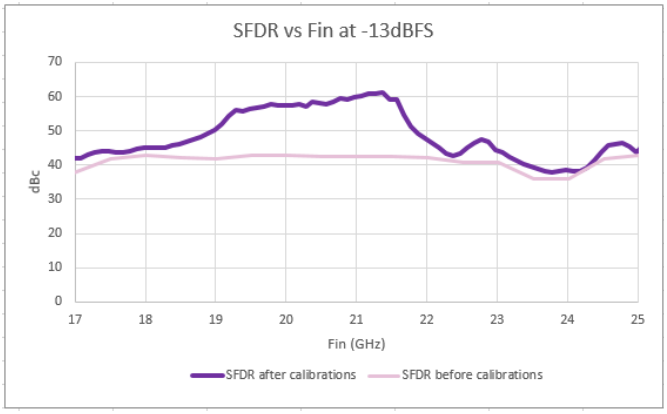

Figure 7 - K-band SFDR pre- and post calibration

TESTING CONCLUSIONS

A stated objective was to evaluate whether reasonable dynamic sampling performance could be attained in the K-band. More specifically, could we achieve a minimum of 50 dBc between 18 to 22 GHz? Despite some early hardware teething problems and some rather disappointing initial results, the methodical approach taken to debug our experimental set-up finally yielded substantial improvements. The final plot (figure 7) shows SFDR performance specifically within our target input frequency range. The results of this work include:

- A demonstrable lift in SFDR between 19.2 and 21.5 GHz of between 15 and 18 dBc peak
- SFDR exceeds 50 dBc between 19 and 21.5 GHz

Inspecting the spectral plot a single tone down converted from 20.478 GHz with the FEB yields the following performance characteristic.

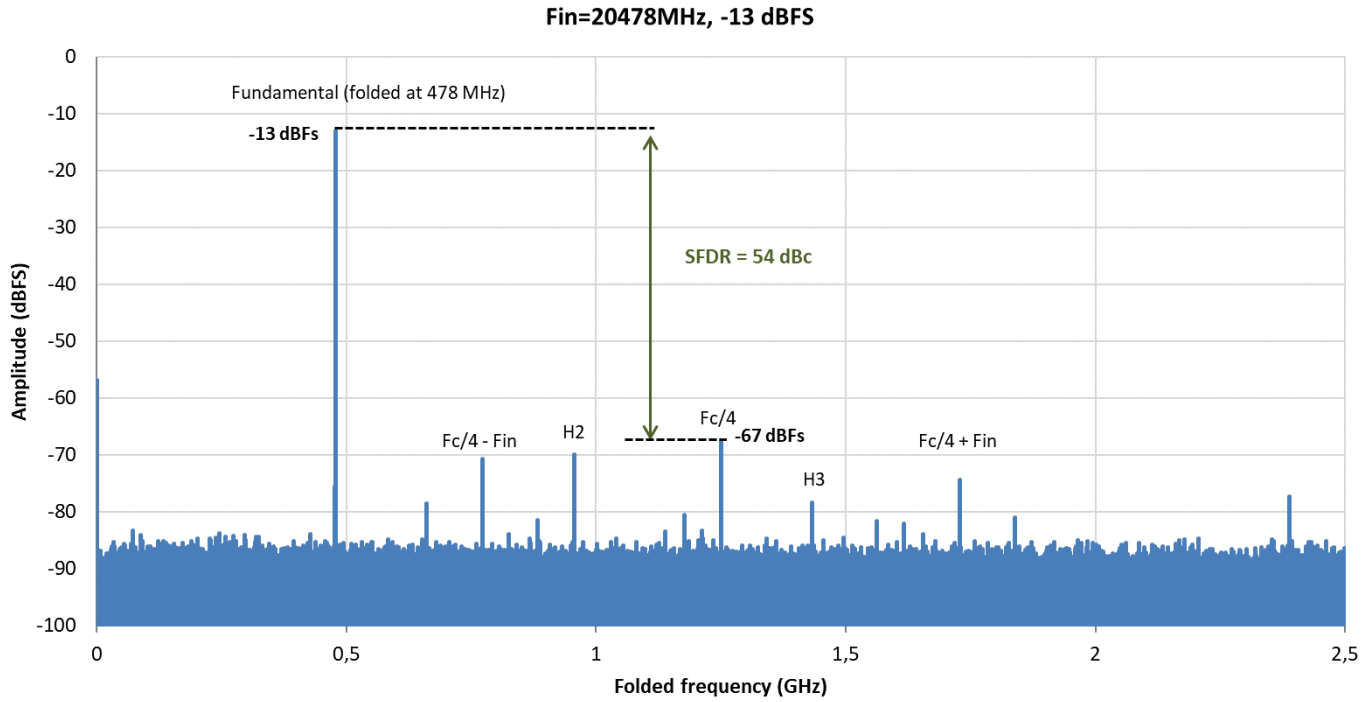

Figure 8 - Spectral plot of 20.478 GHz tone down converted to baseband with the experimental FEB

The results thus far indicate:

- With a -13 dBFS input signal power @ 20.478 GHz we achieve approximately 54 dBc SFDR (figure 13)
- Fc/4 and related spurs still dominate this sampled spectrum (@ -67 dBFS) though all other spurs (Fc/4 ± Fin, H2 & H3) are falling below -69 dBFS
- We have exceeded our minimum 50 dBc SFDR target for this engineering work between 19 and 21.75 GHz

A LOOK TO THE FUTURE

The results discussed in this article were obtained from a prototype FEB, which was known to have several deficiencies. Markedly, there were issues with clock distribution which was suspected to degrade the dynamic performance of the THA. An improved FEB is currently being manufactured and it is expected to offer much better dynamics especially decreasing the H2 spur level. In addition, this board will provide a direct input to bypass the THA for optimum baseband performance. We expect to publish a follow-up review of this experimental work once we have a complete set of further optimized results to report from the new board, which should be available during 2020.

This project represents Teledyne e2v's first steps towards an integrated, direct sampling K-band solution. In addition to offering new capabilities, this has helped us improve engineering skills in this complex domain. The work has helped us gain significant detailed insights into the high frequency optimization of compound, interleaved analogue to digital converter cores especially with respect to high Nyquist zone calibration trade-offs associated with INL & ILG optimization. Overall these lessons will help Teledyne e2v raise the performance bar on future high-end, broadband data convertors.

https://www.teledyne-e2v.com/products/semiconductors/

REFERENCES:

- 1 Teledyne e2v, "Microwave DAC simplifies direct digital synthesis from DC to 26.5 GHz covering X-, Ku-, and K-bands", 2016.
- 2 IEEE Webinar: "12-bit 8 GSps DAC enabling signal generation up to K-band", by R. Pilard. 2019

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