EV10CS140
10-bit 3.0 Gsps 1:4 DMUX

Datasheet

Main Features

- High-speed ADC Family Companion Chip
- 10-bit Data
- Additional 11th Bit in Simultaneous Mode (Example: for Out-of-Range Bit)
- Staggered or Simultaneous Data Outputs
- Selectable 1:4 or 1:2 Demultiplexed Digital LVDS Outputs
- Power Consumption:
  - 2.20 W in 1:4 DMUX Ratio
  - 1.95 W in 1:2 DMUX Ratio
- Power Supplies: V_{CCD} = 3.3V (Digital), V_{PLUSD} = 2.5V (Outputs)

General Features

- LVDS Compatible Differential Data and Clock Inputs (100Ω Terminated)
- LVDS Compatible Differential Data and Data Ready Outputs
- Selectable Active Edge for Output Clocks:
  - Only Rising: DR Mode
  - Rising and Falling: DR/2 Mode
- Clock Input in CLK/2 Mode (Active on Rising and Falling Edge)
- Checker Board Data Frame Generator (BIST)
- Power Management (Sleep Mode)
- EBGA240 (Enhanced Ball Grid Array) Package
- Fine Tuning of Input Clock Path Delay
  - Compensation of External Data and Clock Path Misalignements and Skews
  - Once Tuned, Setting is Valid Over Full Operating Frequency and Over Specified Temperature Range

Screening

- Temperature Range
  - Industrial "V" Grade: –40°C < T_{amb} < 85°C

Applications

This DMUX enables users to process high-speed output data streams from fast analog-to-digital converters down to standard FPGA processor speed.

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1. Description

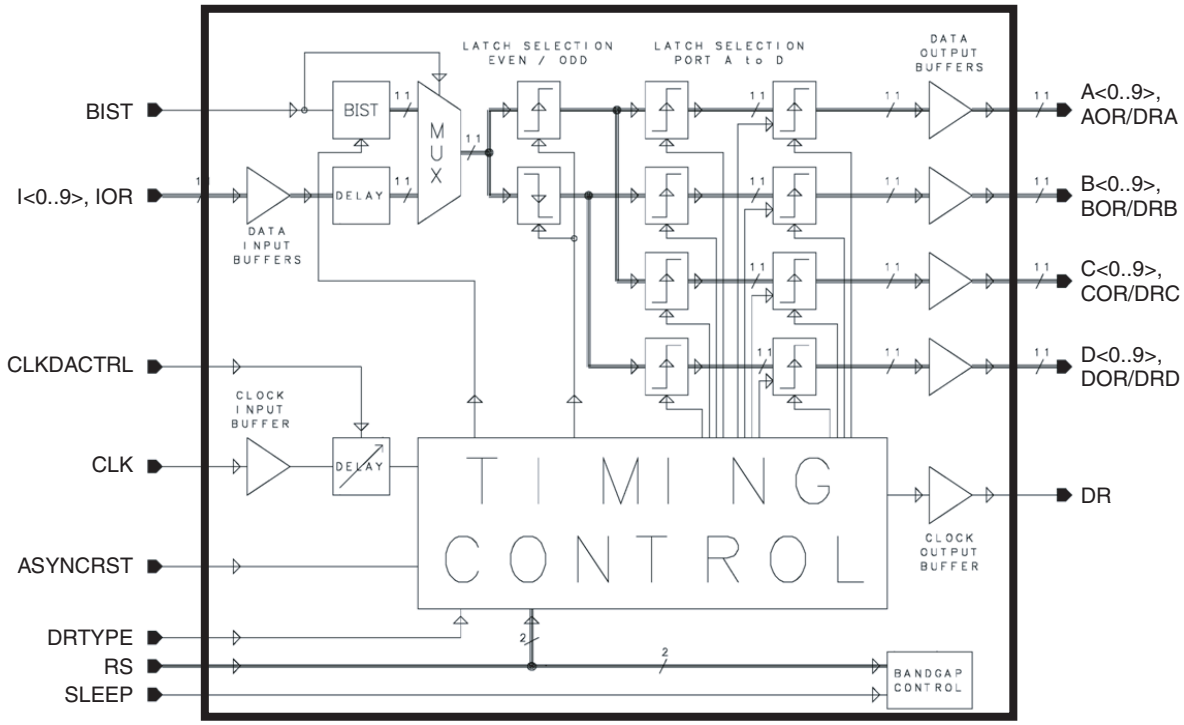
The EV10CS140 is a monolithic high speed-demultiplexer, used to lower a 10-bit data stream of up to 3 Gsps guaranteed rate by a selectable 4 or 2 ratio (a 1:8 ratio might be achieved by interleaving two DMUXes).

The DMUX is a companion chip designed to fit perfectly with all of e2v's high speed ADCs and is capable of tracking the ADC's output sampling rate over all operating frequency and temperature ranges.

Thanks to its LVDS buffers, this DMUX can easily be interfaced with standard high-speed FPGAs (100Ω differentially terminated).

The EV10CS140 has the same pinout and footprint as e2v's AT84CS001 DMUX. No re-design efforts are required to use this low-power DMUX.

Figure 1-1. Block Diagram



2. Functional Description

The EV10CS140 is a monolithic high-speed demultiplexer (DMUX) using high-speed bipolar technology.

It enables the user to lower a 10-bit stream of 3 Gsps minimum by a factor of two or four. The EV10CS140 DMUX can process an Input data rate up to 3Gsps in 1:4 ratio and 1:2 ratio.

The EV10CS140 DMUX is capable of processing an 11-bit data flow (in simultaneous mode). The additional 11th bit (IOR, IORN) might be connected for example to the out-of-range bit of a 10-bit ADC.

The input and output clocks as well as the input and output data are LVDS compatible. Digital inputs are 100Ω differentially terminated on chip. Digital output buffers shall be terminated by a 100Ω differential ASIC load.

The improved architecture of the DMUX facilitates interfacing with high-speed ADCs operating at up to 3 Gsps. Over the full specified clock rate, it is normally not necessary to tune the CLKDACTRL voltage and it is recommended to bias CLKDACTRL pin with $1/3*V_{CCD}$ if the clock is roughly centered within input data. However, a tunable delay cell is integrated in serial with the clock input: it can be used to tune the delay between the data and clock paths namely for high speed rates and in the case of large misalignment or skews between the external clock path and the data path. The delay is controlled by means of the CLKDACTRL analog control input. The tunable delay ranges from –100 ps to 100 ps for CLKDACTRL varying from $1/3*V_{CCD}$ to $2/3*V_{CCD}$.

Two output Data Ready modes can be selected (DR and DR/2) by the means of DRTYPE control input:

- DR mode: only the output clock (DR, DRN) rising edges are active
- DR/2 mode: output clock (DR, DRN) rising and falling edges are active

The input clock has to be in CLK/2 mode (active on rising and falling edges)

The data outputs can be received at the DMUX output in two different modes:

- Staggered: even and odd bits are output with half a data period delay
- Simultaneous: even and odd bits are output at the same time

The EV10CS140 DMUX is started by the ASYNCRST control input that acts as a master asynchronous reset for the device. Once reset, there is no loss of synchronization over an indefinite time period, therefore no additional incoming synchronous reset signal is required.

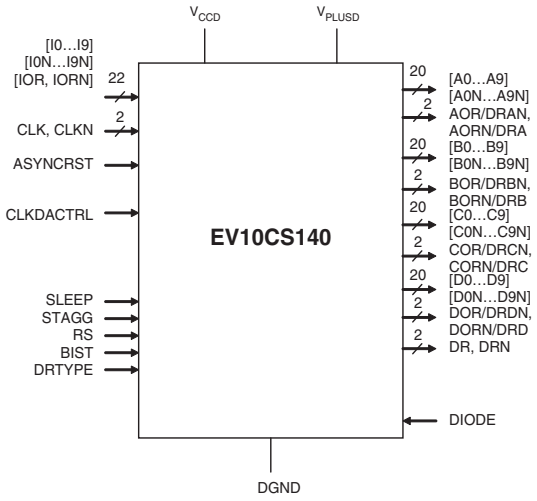
The power consumption of the EV10CS140 is 2.2W in 1:4 mode and 1.95W in 1:2 mode. Power consumption can be reduced at 1.0W by means of the SLEEP control input.

A Built-in Self Test (BIST) is implemented for rapid debugging of the DMUX.

The EV10CS140 DMUX is a companion chip designed to fit perfectly with all of e2v's high-speed ADCs.

Table 2-1. Functional Description

Name	Function
V_{CCD}	Digital 3.3V Power supply
V_{PLUSD}	Output 2.5V Power Supply
DGND	Ground
CLK, CLKN	Input clock signals
I0…I9	In-phase Input data (True)
I0N…I9N	Inverted phase Input data (False)
IOR, IORN	Additional Input bit
DR/DRN	Output clock signals
A0…A9	In-phase Output data Port A
A0N…A9N	Inverted phase Output data Port A
AOR/DRAN, AORN/DRA	Additional Output bit Port A Or Output clock in staggered mode for port A
B0…B9	In-phase Output data Port B
B0N…B9N	Inverted phase Output data Port B
BOR/DRBN, BORN/DRB	Additional Output bit Port B Or Output clock in staggered mode for port B
C0…C9	In-phase Output data Port C
C0N…C9N	Inverted phase Output data Port C
COR/DRCN, CORN/DRC	Additional Output bit Port C Or Output clock in staggered mode for port C
D0…D9	In-phase Output data Port D
D0N…D9N	Inverted phase Output data Port D
DOR/DRDN, DORN/DRD	Additional Output bit Port D Or Output clock in staggered mode for port D
CLKDACTRL	Control signal for Clock Delay cell
ASYNCRST	Asynchronous Reset signal
SLEEP	Sleep mode selection signal
RS	DMUX Ratio selection signal
DRTYPE	Output clock Type selection signal
STAGG	Staggered mode selection for Data outputs
BIST	Built-In Test enable
DIODE	Diode for die Junction Temperature monitoring



Bit 0 corresponds to LSB and Bit 9 to MSB

3. Specifications

3.1 Absolute Maximum Ratings

Table 3-1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Digital power supply	V_{CCD}	3.6	V
Output power supply	V_{PLUSD}	3.6	V
Data Input	I0, I0N…I9, I9N, IOR, IORN	–0.3 to V_{CCD} + 0.3	V
Clock Input	VCLK, VCLKN	–0.3 to V_{CCD} + 0.3	V
Control Inputs	SLEEP, STAGG, RS, ASYNCRST, BIST, DRTYPE, CLKDACTRL	–0.3 to V_{CCD} + 0.3	V
Max Junction Temperature	T_J	125	°C
Storage Temperature	Tstg	–55 to 150	°C
ESD protection (HBM model)	ESD	> 500	V

Notes: 1. Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability.

2. Maximum ratings on I/Os are defined with device powered ON.

3. All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

3.2 Recommended Conditions of Use

Table 3-2. Recommended Conditions of Use

Parameter	Symbol	Comments	Recommended	Unit
Digital power supply	V_{CCD}	No specific power supply sequencing required during power ON / OFF	3.3	V
Output power supply	V_{PLUSD}		2.5	V
Control Inputs	CLKDACTRL		1.1	V
Operating Temperature Range	Top	Industrial grade	$-40 < T_{amb} < 85$	°C

3.3 Electrical Characteristics

Unless otherwise specified, the specification below apply over full temperature and power supply range.

Table 3-3. Electrical Characteristics

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Resolution		4	10 bit with additional 11th bit			Bit
Power Requirements						
Digital power supply voltage	V_{CCD}	1	3.15	3.3	3.45	V
Output power supply voltage	V_{PLUSD}	1	2.375	2.5	2.625	V
Digital power supply current 1:2 mode 1:4 mode SLEEP mode (1:4 or 1:2) 1:2 mode with BIST enabled 1:4 mode with BIST enabled	I_{VCCD}	1		 385 440 135 360 415	 450(1) 510(1) 170(1) 420(1) 480(1)	mA
Output power supply current 1:2 mode 1:4 mode SLEEP mode (1:4 or 1:2)	I_{VPLUSD}	1		 270 300 240	 410(1) 440(1) 370(1)	mA
Power dissipation 1:2 mode 1:4 mode SLEEP mode (1:4 or 1:2) 1:2 mode with BIST enabled 1:4 mode with BIST enabled	P_D	1		 1.95 2.2 1.1 1.85 2.1	 2.6(1) 2.9(1) 1.5(1) 2.5(1) 2.8(1)	W
LVDS Data/Clock Inputs and Outputs						
Logic Compatibility			LVDS			
Input Common Mode(2)	V_{ICM}	1	1	1.25	1.6	V
Output Common Mode(3)	V_{OCM}	1	1.125	1.25	1.425	V
Differential input (2)	V_{IDIFF}	1	100	350	–	mV
Differential output	V_{ODIFF}	1	250	350	450	mV
Output level “High” (4)	V_{OH}	1	1.25	1.425	–	V
Output level “Low”(4)	V_{OL}	1	–	1.075	1.25	V
STATIC Inputs (SLEEP, STAGG, BIST, RS, DRTYPE)						
Control Input Voltages and currents: - Logic low Resistor to ground Voltage level Input low current - Logic high Resistor to ground Voltage level Input high current	 R_{IL} V_{IL} I_{IL} R_{IH} V_{IH} I_{IH}	1	 0 0 –500 10k 2.0		 10 0.5 Infinite V_{CCD} 10	 Ω V µA Ω V µA
STATIC Inputs (CLKDACTRL)						

Table 3-3. Electrical Characteristics (Continued)

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Control Input Voltages		4	V_{CCD} / 3		$2 \times V_{CCD}$ / 3	V
RESET Input (ASYNCRST)						
Logic Compatibility			LVCMOS/CMOS			
Reset input voltages and currents - Logic Low	 V_{IL} I_{IL}	 1	 0 –300		 1.4	 V µA
- Logic High	V_{IH} I_{IH}		1.8		V_{CCD} 50	V µA

Notes: 1. Worst case value obtained with maximum supply voltages over full temperature range.
2. Given for a differential input.
3. Assuming 100Ω termination ASIC load.
4. V_{OH} min and V_{OL} max can never be at 1.25V at the same time, with respect to V_{ODIFF} min = 250 mV

Table 3-4. Switching Performances and Characteristics

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Input Clock						
Input Clock duty cycle	DCYC	4	35	50	65	%
Maximum Input Clock Frequency DR TYPE= DR/2, RS = 1:2 DR TYPE= DR/2, RS = 1:4 DR TYPE= DR, RS = 1:2 DR TYPE= DR, RS = 1:4	Fclk	4	 1.5 1.5 1.5 1.5			GHz
Input Data						
Data to Input Clock setup & hold time(1)	Tsetup/THold	4				ps
Maximum Input Data Rate DR TYPE= DR/2, RS = 1:2 DR TYPE= DR/2, RS = 1:4 DR TYPE= DR, RS = 1:2 DR TYPE= DR, RS = 1:4	Fs	4	 3.0 3.0 3.0 3.0			Gsps
Output Data						
Maximum Output Data Rate DR TYPE= DR/2, RS = 1:2 DR TYPE= DR/2, RS = 1:4 DR TYPE= DR, RS = 1:2 DR TYPE= DR, RS = 1:4		4	 1.5 0.75 1.5 0.75			Gsps
Output Rise/Fall time for Data (20% – 80%)(2)	TR/TF	4		120/120	180/180	ps
Output Rise/Fall time for Data Ready (20% – 80%)(2)	TR/TF	4		120/120	180/180	ps
CLK to Data Output delay	TOD	4	2.20	2.30	2.40	ns
CLK to Data Ready Output delay	TDR	4	2.10	2.15	2.20	ns
Data Ready to Data delay	TOD – TDR	4	100	150	200	ps

Table 3-4. Switching Performances and Characteristics (Continued)

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Output Data Pipeline delay: Synchronized 1:2 mode Synchronized 1:4 mode Staggered 1:2 mode Staggered 1:4 mode	PD_D	4		 0.5 1.5 0 / 0.5 0 / 0.5 / 1 / 1.5		Clock Cycles
CLK to Output Data Ready delay: Synchronized 1:2 mode Synchronized 1:4 mode Staggered 1:2 mode Staggered 1:4 mode	PD_DR	4		 1.0 2.5 0.5 / 1.0 1 / 1.5 / 2 / 2.5		Clock Cycles
Asynchronous Reset						
ASYNCRST minimum pulse width	RSTPW	5		3		ns
CLK to ASYNCRST timing[3] Forbidden area width Minimum delay between falling edge of ASYNCRST and rising edge of CLK		 4 4			 250 ±125	 ps ps

Notes:
1. Input data to input clock setup and hold time are not defined, because they are dependent of CLKDACTRL adjustment. It is recommended to center the clock edge in the middle of the data (with ± 100 ps) and to adjust CLKDACTRL to 1.1V (1/3 of V_{CCD}).
2. Rise time and fall time are defined for an output load of 2 pF.
3. See Figure 4-1 on page 9, CLK to ASYNCRST timing is given assuming V(CLKDACTRL) = 1.1V

3.4 Explanation of Test Levels

Table 3-5. Test Levels

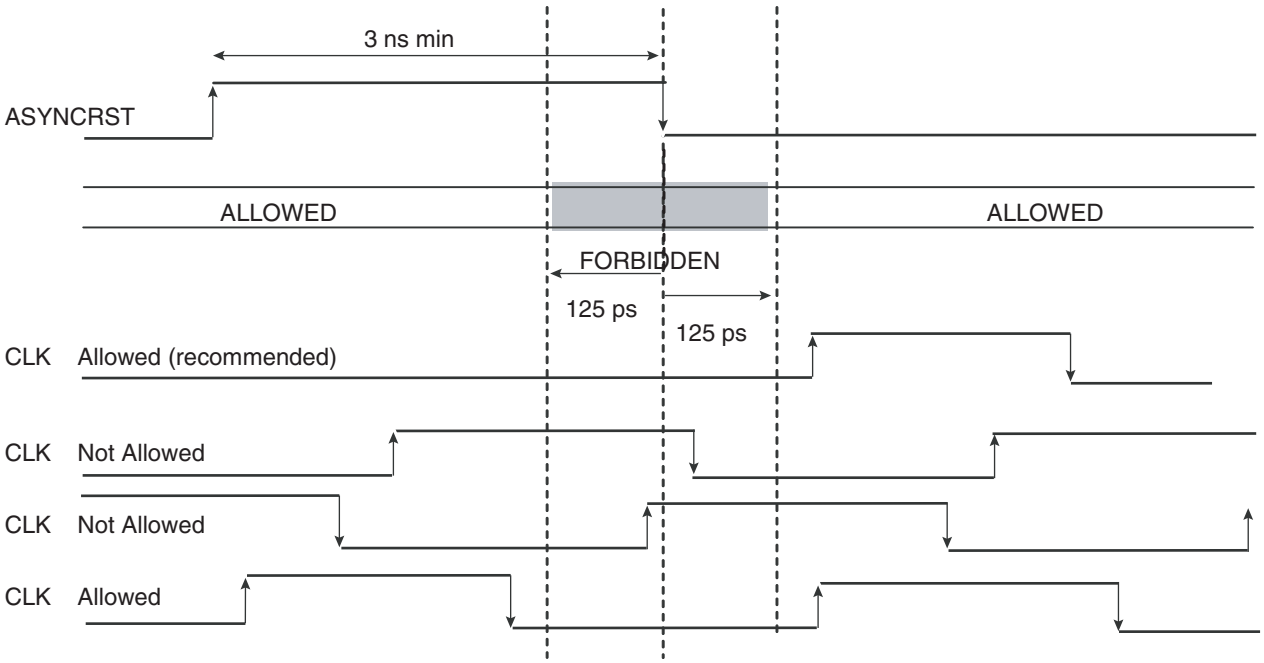
1	100% production tested at +25°C
2	100% production tested at +25°C, and sample tested at specified temperature
3	Sample tested only at specified temperature
4	Parameter is guaranteed by design and characterization testing (thermal steady-state conditions at specified temperature)
5	Parameter is a typical value only

Only MIN and MAX values are guaranteed (typical values are issuing from characterization results).

The level 1 and 2 tests are performed at 100 MHz

4. Timing Diagrams

Figure 4-1. CLK to ASYNCRST Timing with V(CLKDACTRL) = 1.1V



It is highly recommended to stop the clock at the Low level when ASYNCRST is active (high level). Note that when e2v's ADCs are in reset, the ADC Data Ready output (input clock of the DMUX) is stopped at the low level. In the case where the clock can not be stopped during the reset (note recommended), it is not allowed to have an active edge (rising and falling edge) of the CLK clock within a ±125 ps area around the falling edge of ASYNCRST.

The end of the reset occurs at the falling edge of ASYNCRST, and the edge of the Clock has to occur at the minimum 125 ps after the falling edge of ASYNCRST to ensure a proper timing.

The figure presented above is given for V(CLKDACTRL) = 1/3*V_{CCD} = 1.1V. If V(CLKDACTRL) has a different value, the forbidden area has to be shifted accordingly to V(CLKDACTRL) value. Please refer to Figure 5-9 on page 18 for delay calculation.

For example, assuming ambient temperature and typical supplies, if V(CLKDACTRL) is set to 1.65V, the delay compared to 1.1V is 95 ps – 0 ps = 95 ps. This means that it is forbidden to have an active edge of the clock within –220 ps / 30 ps (the forbidden area is shifted on the left of the above figure).

Figure 4-2. Simultaneous 1:2 Mode – DRTYPE = DR/2

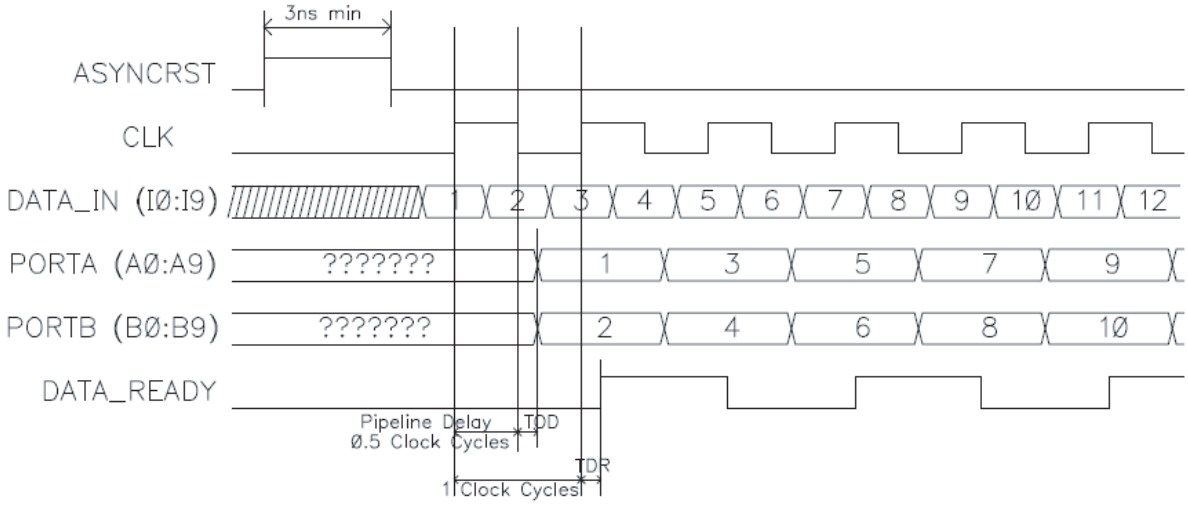


Figure 4-3. Simultaneous 1:4 Mode – DRTYPE = DR/2

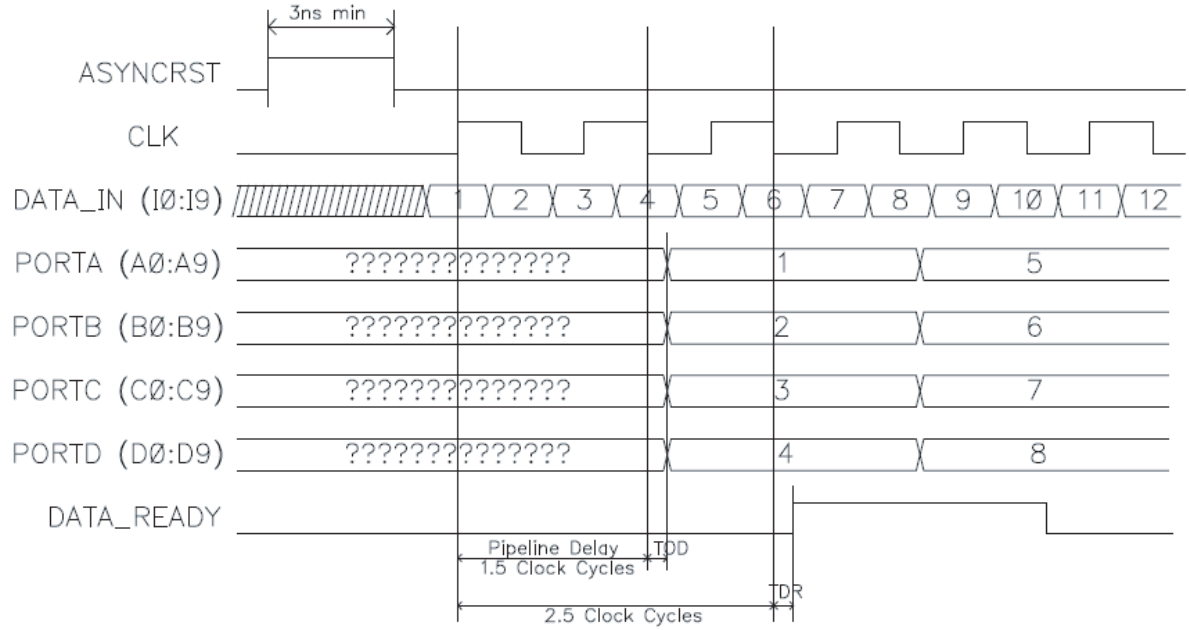
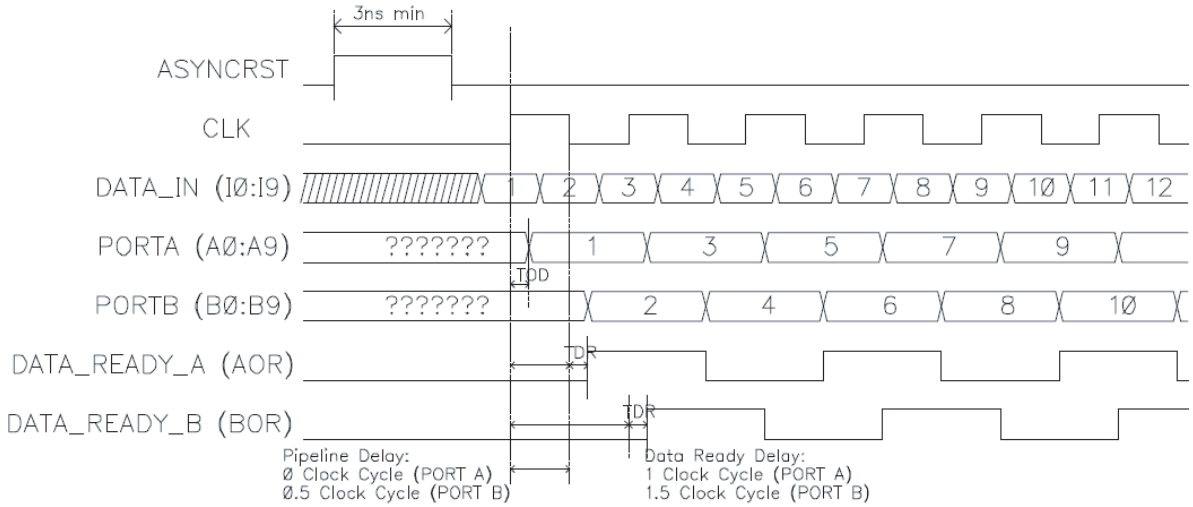
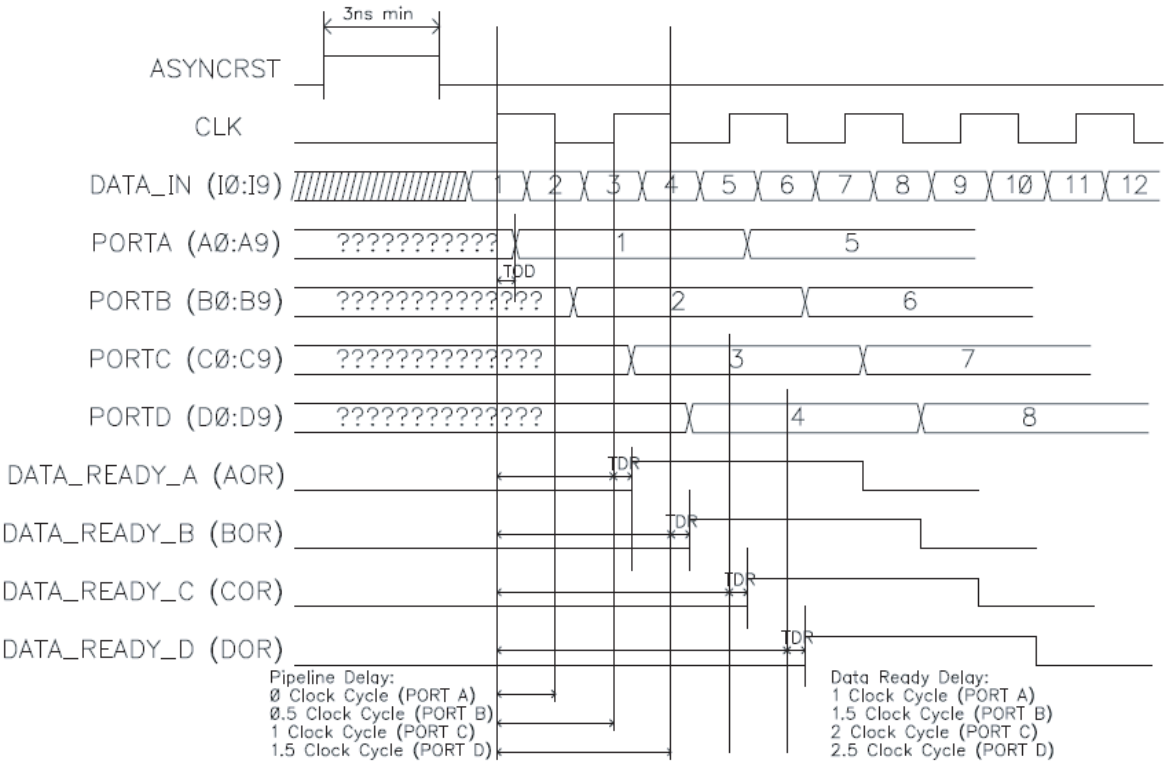


Figure 4-4. Staggered 1:2 Mode – DRTYPE = DR/2



Note: DATA_READY A = DRA (pin A6)
DATA_READY B = DRB (pin H1)

Figure 4-5. Staggered 1:4 Mode – DRTYPE = DR/2



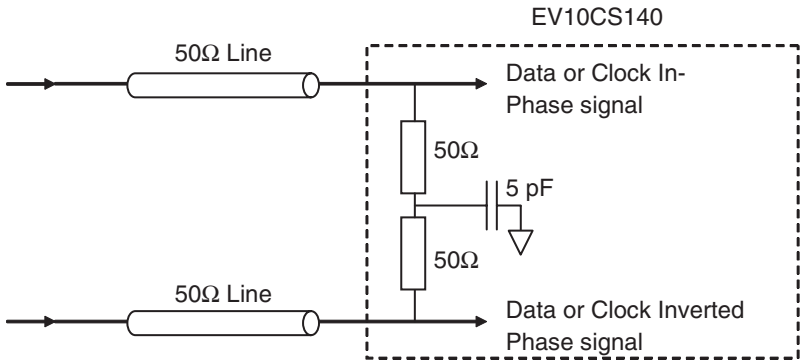
Note: DATA_READY A = DRA (pin A6)
DATA_READY B = DRB (pin H1)
DATA_READY C = DRC (pin W5)
DATA_READY D = DRD (pin W16)

5. Description of Main Functions

5.1 LVDS Input Data and Clock

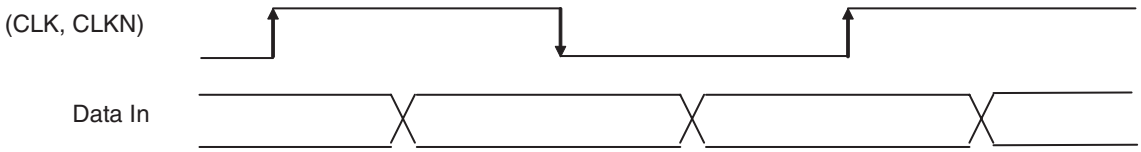
Input data (I0, I0N…I9, I9N and IOR, IORN) and clock (CLK, CLKN) are LVDS compatible. They are 2 × 50Ω differentially terminated inside the chip as described in Figure 5-1 on page 12. (No need to add external terminated resistors).

Figure 5-1. EV10CS140 LVDS Input Data and Clock Termination Scheme



The input clock has to be used in CLK/2 mode (active on rising and falling edge).

Figure 5-2. Clock Active on Falling and Rising Edge



5.2 Additional Bit (IOR,IORN)

Differential inputs IOR, IORN can be used in simultaneous mode only (not in staggered mode).

When a signal is applied on IOR and IORN, the “additional bit” is activated. It can be used to process the Out of Range bit from the ADC, in which case, the DMUX features an 11-bit input/output data stream.

IOR, IORN is demultiplexed by the selected DMUX ratio:

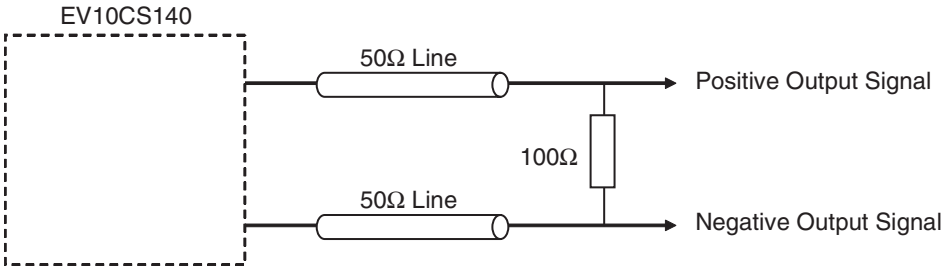
- In 1:4 ratio, the 11th bit is outputted on AOR/DRAN, AORN/DRA, BOR/DRBN, BORN/DRB, COR/DRCN, CORN/DRC and DOR/DRDN, DORN/DRD at a quarter of its initial speed.
- In 1:2 ratio, the 11th bit is outputted on AOR/DRAN, AORN/DRA and BOR/DRBN, BORN/DRB at half its initial speed.

Note: In Staggered output mode:
(AORN/DRA, AOR/DRAN), (BORN/DRB, BOR/DRBN), (CORN/DRC, COR/DRCN) and (DORN/DRD, DOR/DRDN) are used as the Data Ready signal (output clock) for each port.
In this mode the additional bit is disabled.

5.3 LVDS Output Data and Clocks

The data (Ax, AxN…Dx, DxN, AOR/DRAN, AORN/DRA…DOR/DRDN and DORN/DRD) and clock outputs (DR, DRN) are LVDS compatible. They must be 100Ω differentially terminated as close as possible to the differential receiver as described in Figure 5-3.

Figure 5-3. EV10CS140 LVDS Output Termination Scheme



Note: in 1:2 DMUX Ratio, the unused outputs of Port C and D can be left floating. Refer to Section 5.5 ”Programmable DMUX Ratio” on page 14.

5.4 Control Signal Settings

The SLEEP, RS, STAGG, BIST and DRTYPE control signals use the same input buffer.

SLEEP, STAGG, BIST are activated on Logic Low (10 Ohms Grounded or tired to GND), and deactivated on Logic High (10 KΩ to Ground, or tied to V_{CCD} = 3.3V, or left floating).

Figure 5-4. Control Signal Settings (SLEEP, RS, STAGG, BIST and DRTYPE)

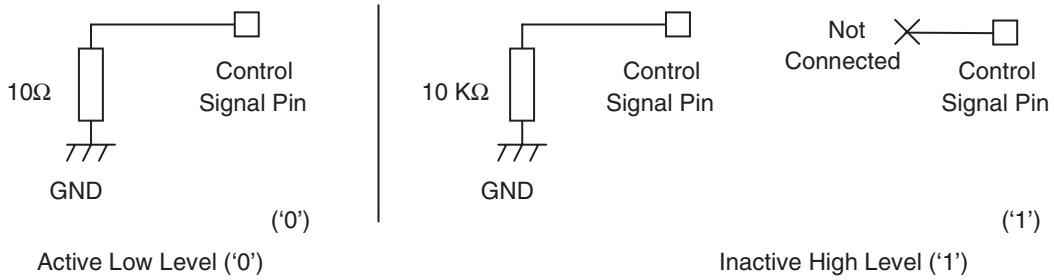


Table 5-1. DMUX Mode Settings – Summary

Function	Logic Level	Electrical Level		Description
		Static drive	Dynamic drive(1)	
BIST	0	10Ω to ground	V(BIST) ≤ V_{IL}	BIST (Checker Board generator)
	1	10 KΩ to ground	V(BIST) ≥ V_{IH}	Normal conversion
		N/C		
SLEEP	0	10Ω to ground	V(SLEEP) ≤ V_{IL}	Power reduction mode (the outputs are fixed at an arbitrary LVDS level)
	1	10 KΩ to ground	V(SLEEP) ≥ V_{IH}	Normal conversion
		N/C		

Table 5-1. DMUX Mode Settings – Summary (Continued)

Function	Logic Level	Electrical Level		Description
		Static drive	Dynamic drive[1]	
STAGG	0	10Ω to ground	V(STAGG) ≤ V_{IL}	Staggered mode
	1	10 KΩ to ground	V(STAGG) ≥ V_{IH}	Simultaneous mode
		N/C		
RS	0	10Ω to ground	V(RS) ≤ V_{IL}	1:2 ratio
	1	10 KΩ to ground	V(RS) ≥ V_{IH}	1:4 ratio
		N/C		
DRTYPE	0	10Ω to ground	V(DRTYPE) ≤ V_{IL}	DR/2 mode
	1	10 KΩ to ground	V(DRTYPE) ≥ V_{IH}	DR mode
		N/C		

Note: 1. Refer to Table 3-3 on page 6 for logical levels.

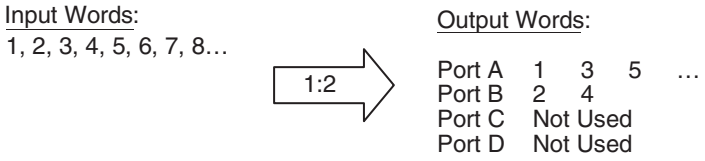
5.5 Programmable DMUX Ratio

The demultiplexer ratio is programmable thanks to the RS Ratio selection signal:

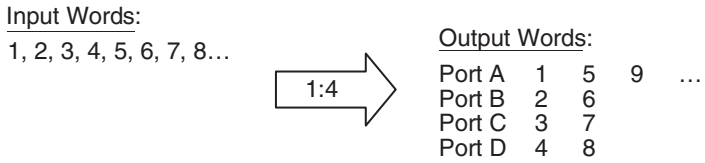
Table 5-2. DMUX Ratio Selection Settings

RS	DMUX Ratio
0	1:2
1	1:4

DMUX in 1:2 Ratio



DMUX in 1:4 Ratio



Note: in 1:2 mode, unused Port C & D can be left floating.

5.6 Data Ready DRTYPE Selection

Two modes for the output clock type can be selected by the means of the DRTYPE single-ended digital input.

For proper logic 1 or 0 settings, refer to section Table 3-3 on page 6.

- When DRTYPE is at logic “1”, the DMUX is in DR mode for output clocks - only the rising edges of the output clocks are active.
- When DRTYPE is at logic “0”, the DR/2 mode is activated for output clocks: both the rising and falling edges of the output clocks are active.

Notes: The preferred (and recommended) mode is DR/2.

Table 5-3. DMUX Output Clock Type Selection Logical Settings

DRTYPE	DMUX Output Clock Type
1	DR
0	DR/2

5.7 Output Mode (STAGG)

Two output modes are provided:

- Staggered: the data packets are output one after the other.
- Simultaneous: all the data packets are output at the same time.

In staggered mode, the output clock for each port is provided by the DRA, DRAN, DRB, DRBN, DRC, DRCN and DRD, DRDN signals, which corresponds to AORN, AOR, BRON, BOR, CORN, COR, DORN and DOR respectively.

The Simultaneous mode is the default mode (STAGG left floating or at logic “1”). The Staggered mode is activated by the means of the STAGG input (active low level).

Figure 5-5. Simultaneous Mode in 1:4 ratio (STAGG = 1)

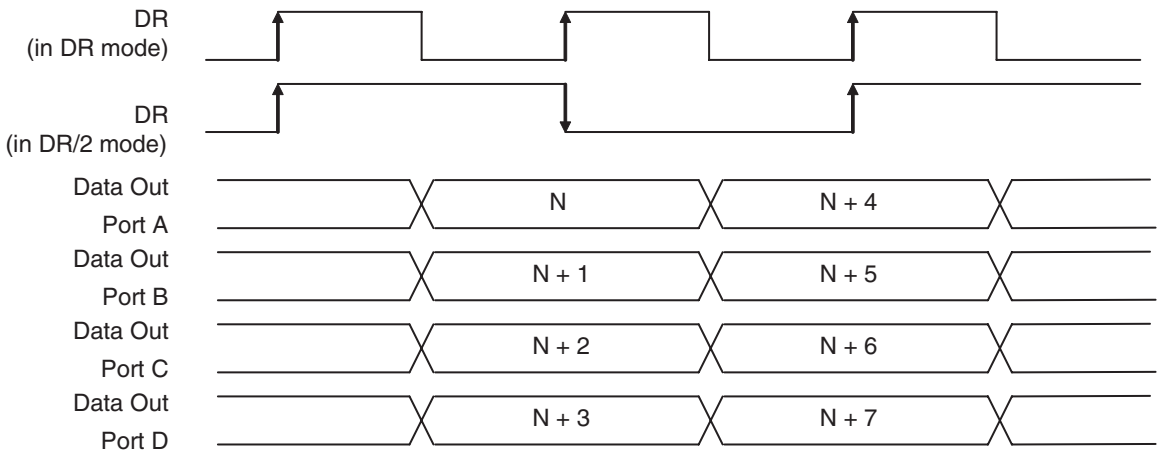


Figure 5-6. Staggered Mode in 1:2 ratio (STAGG = 0)

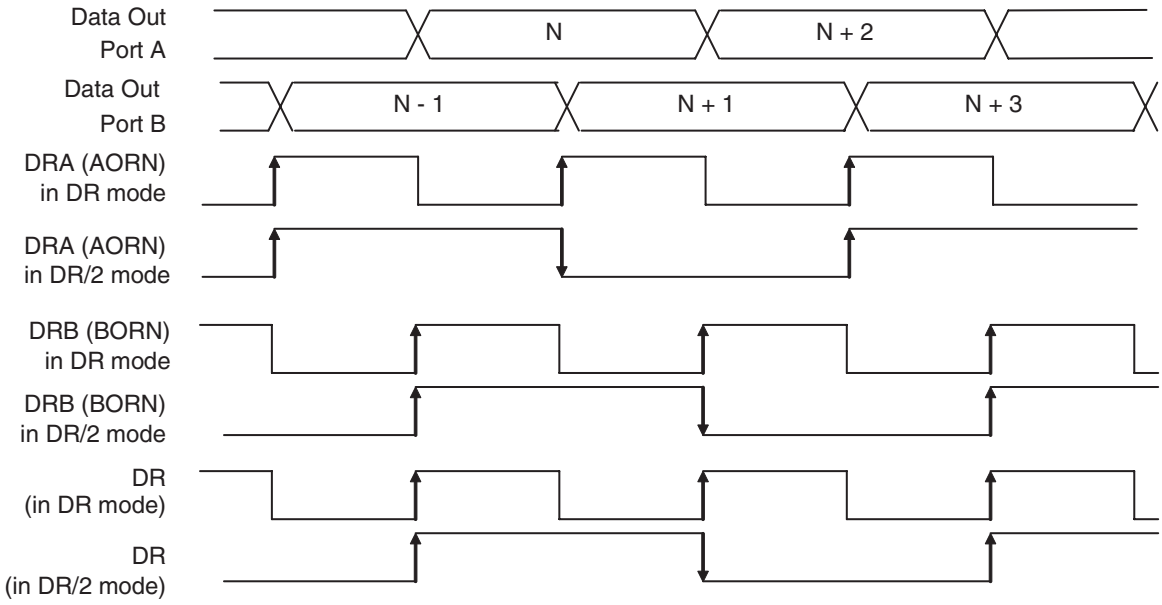
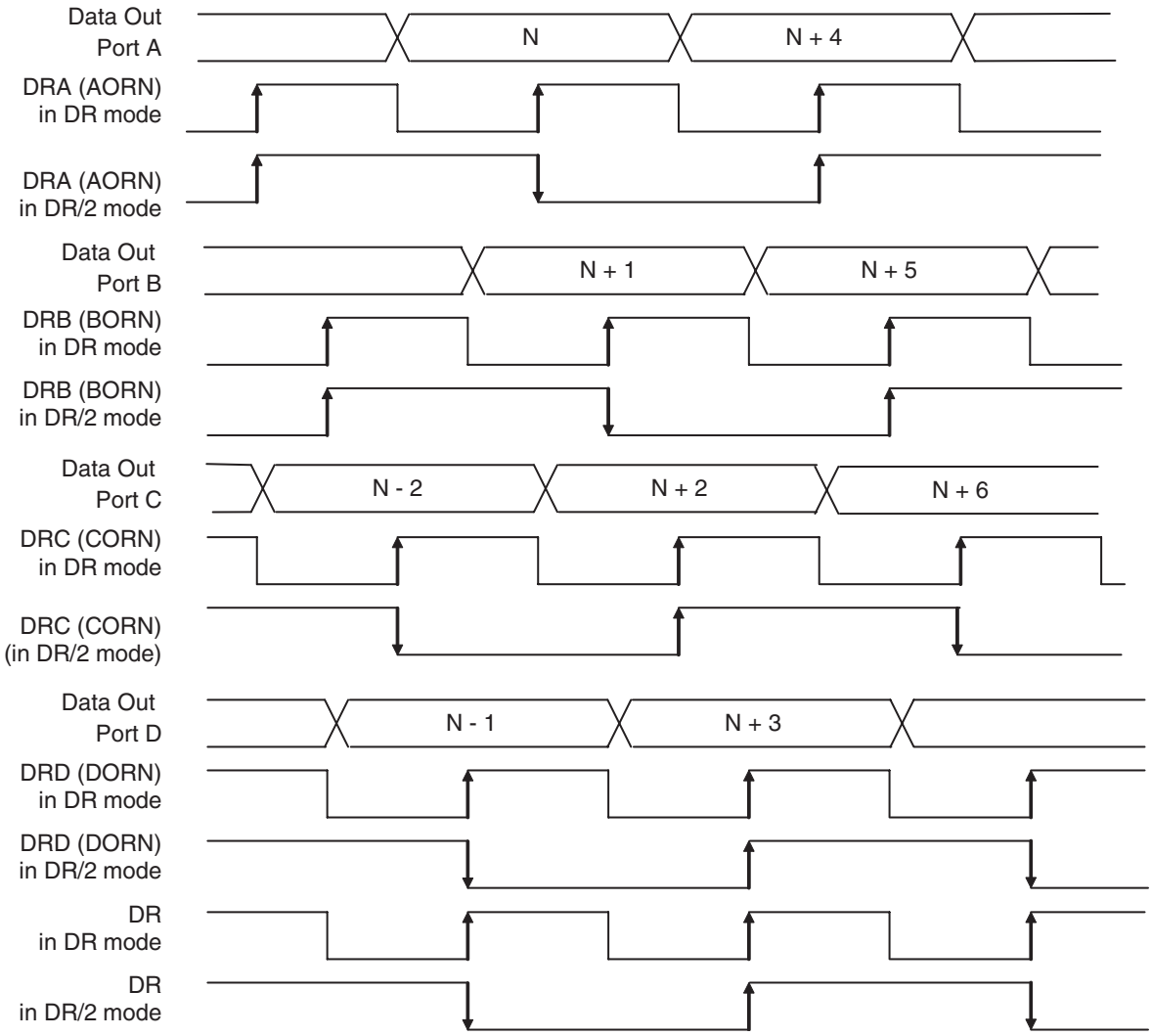


Figure 5-7. Staggered Mode in 1:4 Ratio (STAGG = 0)



5.8 Asynchronous Reset (ASYNCRST)

The ASYNCRST asynchronous reset input is required to start/initialize the device, and acts as a master reset of the DMUX.

ASYNCRST is activated on Logic HIGH (tied/switched to V_{CCD} = 3.3V), and deactivated on Logic LOW (Grounded). Refer to section Table 3-3 on page 6 for logical levels.

During the asynchronous reset, the DMUX' differential clock input (CLK, CLKN) of the DMUX should be stopped at low level (state in which the e2v's single ADC Data Ready signals are when the ADC is in reset).

The ASYNCRST pulse should be last at least 3 ns.

An asynchronous reset is mandatory in order to have a deterministic output data sequence in BIST mode.

5.9 Power reduction Mode (SLEEP)

The Power reduction mode saves up to 50% of power consumption. In this mode, the DMUX delivers an arbitrary digital output pattern with LVDS logic states (no toggling).

The Power Reduction mode is enabled by the SLEEP input. SLEEP is activated on logic LOW (grounded), and deactivated on logic HIGH (10 KW to Ground, or tied to V_{CCD} = 3.3V, or left floating).

5.10 Clock Input Delay Cell (CLKDACTRL)

A fine tune delay cell is provided to fine-tune the delay between the clock path and the data path at the DMUX input. This adjustment may be necessary depending on the sampling rate and/or if there are mis-alignments or skews on the different input data. However, data path skews should be maintained below 50 ps.

The delay is controlled by the means of the CLKDACTRL Analog control input. It ranges from –100 ps to 100 ps for CLKDACTRL varying from $1/3*V_{CCD}$ to $2/3*V_{CCD}$.

This delay depends on the center position of (CLK, CLKN) Clock path in relation to the digital input data in the DMUX input data paths (I0, I0N) …(I9, I9N) and (IOR, IORN).

It is recommended to bias CLKDACTRL pin with $1/3*V_{CCD}$ assuming DEMUX input clock is centered within input data.

Figure 5-8. Block Diagram of the Clock Input Delay Cell

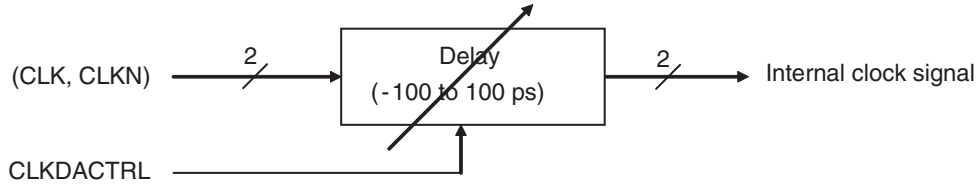
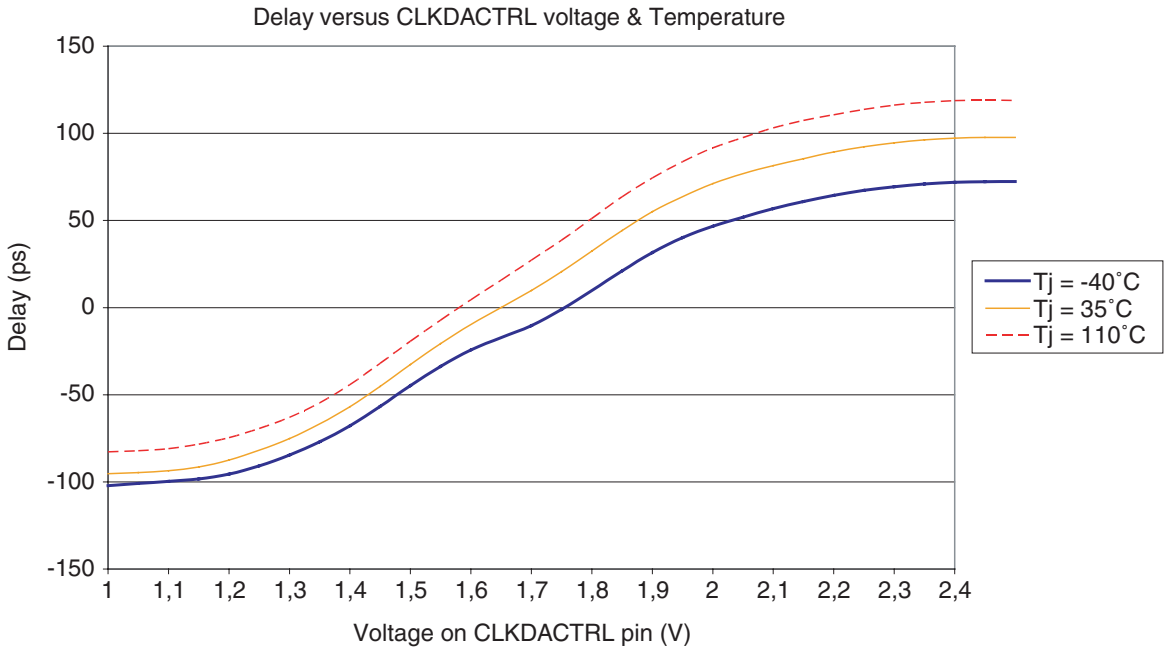
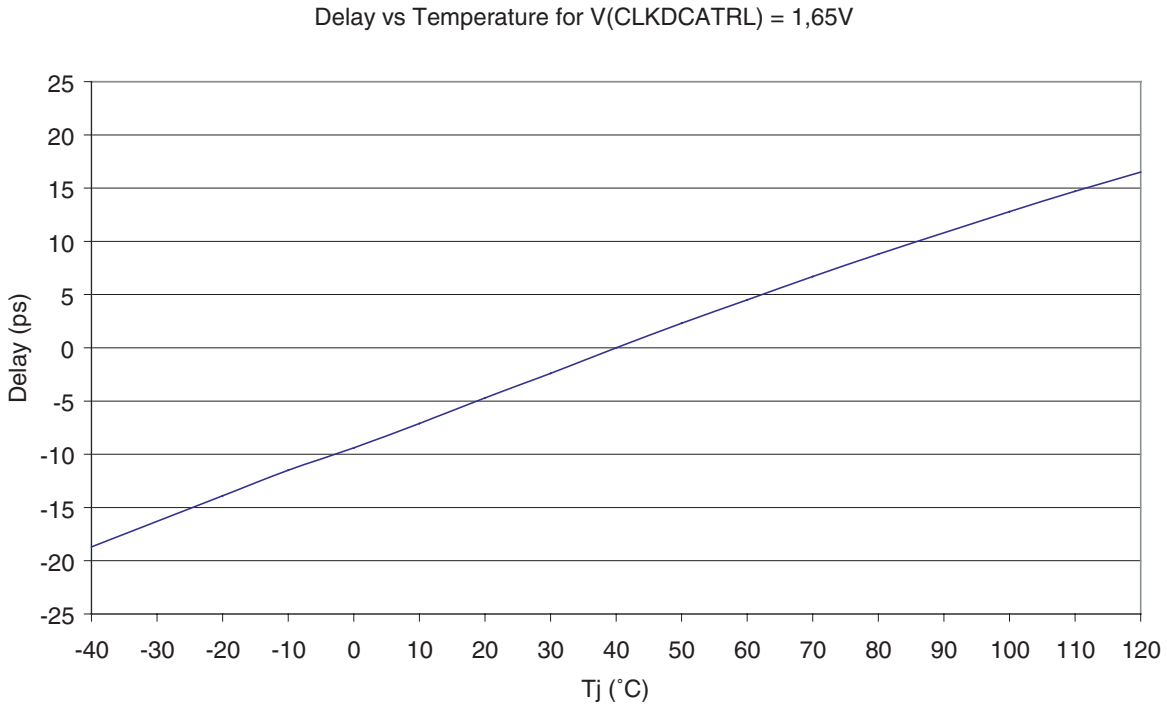


Figure 5-9. CLKDACTRL Transfer Characteristics of the Delay Cell



The tuning range is varying linearly over the specified temperature range. The longest tuning range is obtained at hot temperature.

Figure 5-10. CLKDACTRL Delay Cell Tuning Range vs. T_J



5.11 Built-In Test (BIST)

A Checker Board Pattern might be activated by the means of the BIST input. The BIST is activated on logic LOW (grounded), and deactivated on logic HIGH (10 KΩ to Ground, or tied to V_{CCD} = 3.3V, or left floating).

When activated, the digital outputs correspond to a sequence of “0” and “1”. Each bit is toggling at the clock rate. In order to have a deterministic output sequence, it is necessary to perform an asynchronous reset. The output sequence is then:

Table 5-4. BIST Output Sequence in 1:4 DMUX Ratio

BIST sequence	Binary (D9 …. D0)	Hexa (D9…D0)	Binary 11th bit
Port A	10 1010 1010	0x2AA	0
Port B	01 0101 0101	0x155	1
Port C	10 1010 1010	0x2AA	0
Port D	01 0101 0101	0x155	1
Port A	01 0101 0101	0x155	1
Port B	10 1010 1010	0x2AA	0
Port C	01 0101 0101	0x155	1
Port D	….	…	…

5.12 DMUX Die Junction Temperature Monitoring

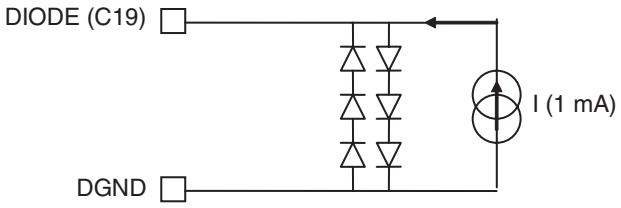
If not used the die junction temperature can be left floating or connected to ground.

A die junction temperature measurement setting is available, for maximum junction temperature monitoring (hot point measurement).

The measurement method consists in forcing a 1 mA current into a diode mounted transistor and sensing the voltage across the DIODE pin and the closest available ground pin.

The measurement setup is described in the Figure hereafter:

Figure 5-11. DMUX Diode for Die Junction Temperature Monitoring Setup



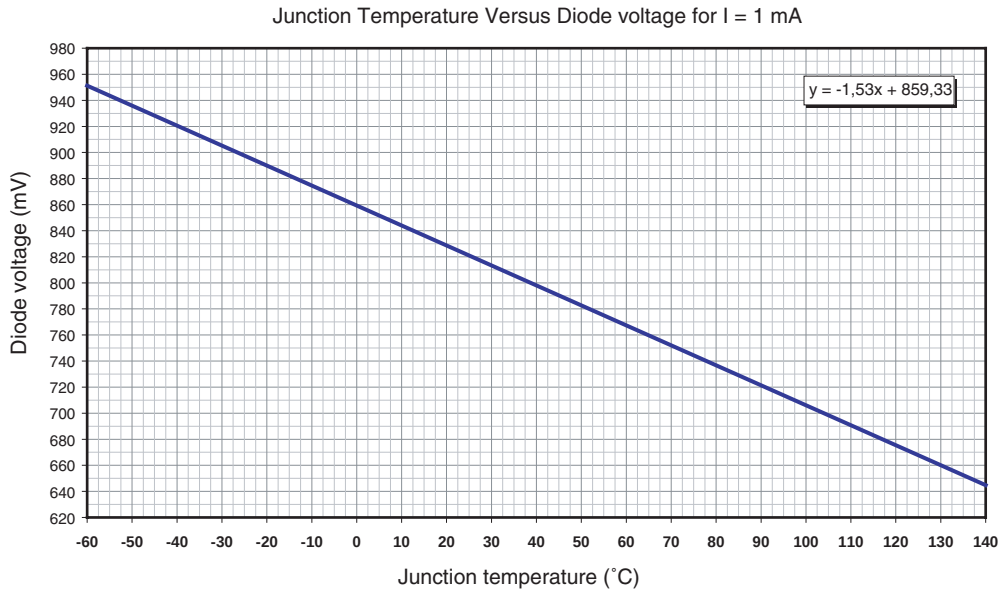
CAUTION:

Respect the current source polarity.

In all cases, make sure that the maximum voltage compliance of the current source is limited to a maximum of 1V or use a resistor mounted in series with the current source to avoid damages, which may occur to the transistor device (this may occur for instance if the current source is connected in reverse).

The forward voltage drop (V_{DIODE}) across diode component, versus junction temperature, (including chip parasitic resistance), is given below (I_{DIODE} = 1mA).

Figure 5-12. Junction Temperature Diode Characteristics

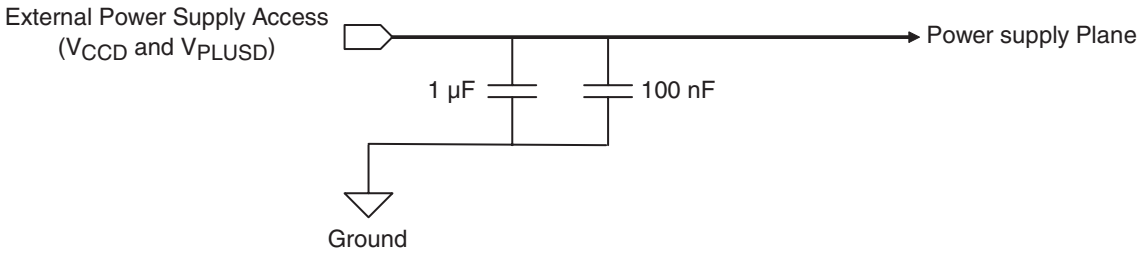


6. Applying the EV10CS140

6.1 Bypassing, Decoupling and Grounding

All power supplies have to be decoupled to Ground as close as possible to the signal accesses to the board by 1 µF in parallel to 100 nF.

Figure 6-1. EV10CS140 Power Supplies Decoupling and Grounding Scheme

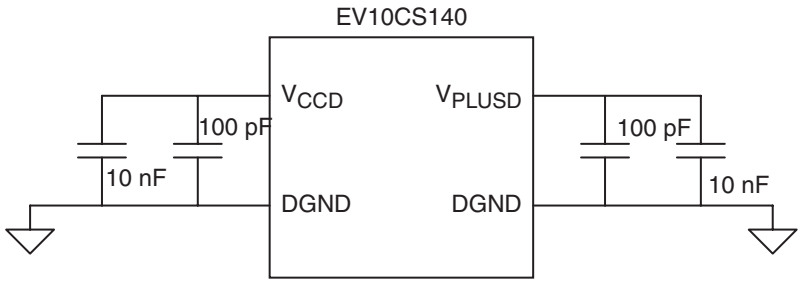


Each group of neighboring power supply pins attributed to the same value should be bypassed with at least one pair of 100 pF in parallel to 10 nF capacitors. These capacitors should be placed as close as possible to the power supply package pins.

The minimum required pairs of capacitors by power supply type is:

- 15 for V_{CCD}
- 14 for V_{PLUSD}

Figure 6-2. EV10CS140 Power Supplies Bypassing Scheme



7. Pin Description

Table 7-1. Pin Description

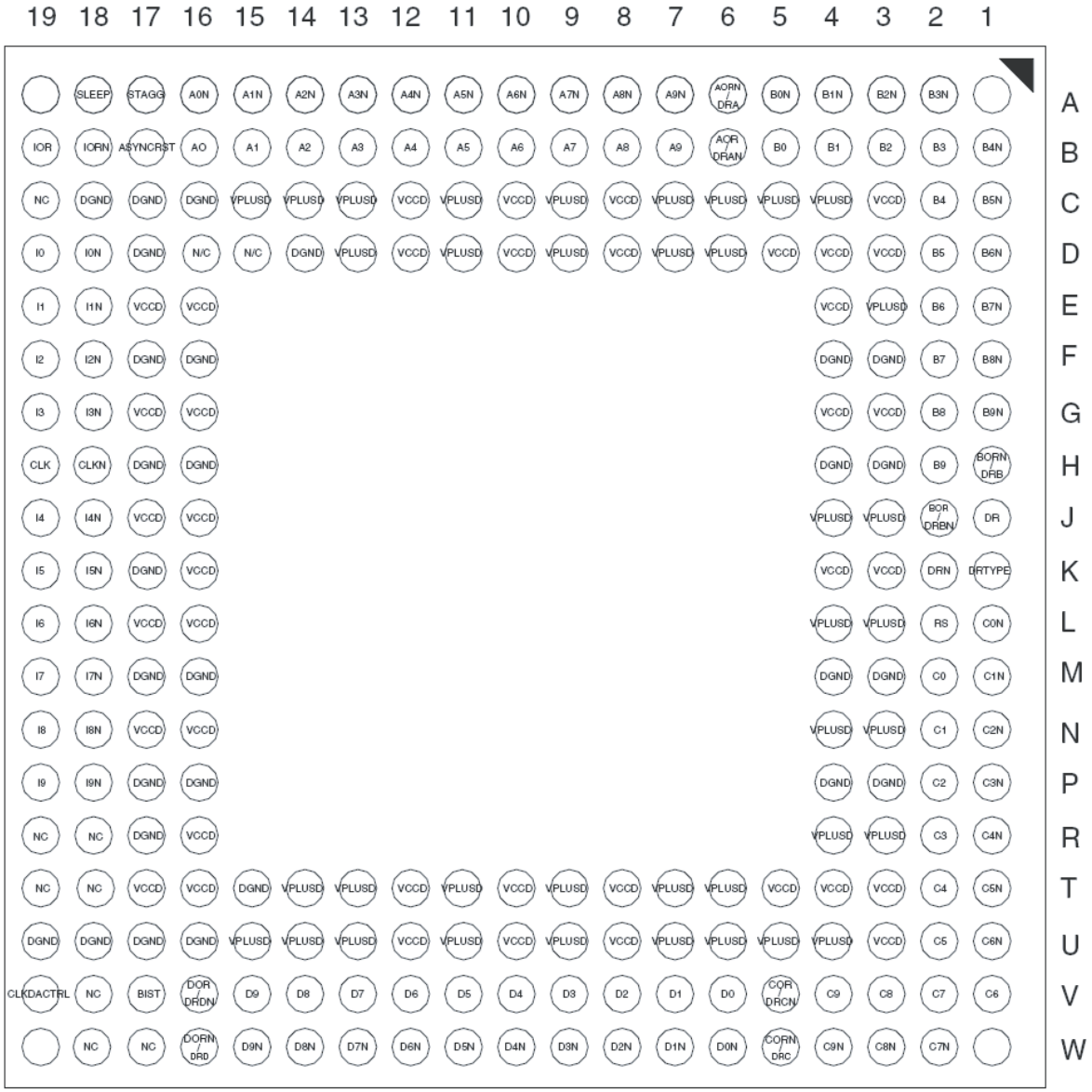
Symbol	Pin Number	Function
POWER SUPPLIES		
V_{CCD}	C12, C10, C8, C3, D12, D10, D8, D5, D4, D3, E4, E17, E16, G17, G16, G4, G3, J17, J16, K16, K4, K3, L17, L16, N17, N16, R16, T17, T16, T12, T10, T8, T5, T4, T3, U12, U10, U8, U3	Output 3.3V supply
V_{PLUSD}	C15, C14, C13, C11, C9, C7, C6, C5, C4, D13, D11, D9, D7, D6, E3, J4, J3, L4, L3, N4, N3, R4, R3, T14, T13, T11, T9, T7, T6, U15, U14, U13, U11, U9, U7, U6, U5, U4	Output 2.5V supply
DGND	C18, C17, C16, D17, D14, F17, F16, F4, F3, H17, H16, H4, H3, K17, M17, M16, M4, M3, P17, P16, P4, P3, R17, T15, U19, U18, U17, U16	Ground
Digital Inputs		
I0, I1, I2, I3, I4, I5, I6, I7, I8, I9	D19, E19, F19, G19, J19, K19, L19, M19, N19, P19	In-phase (+) digital input signal
I0N, I1N, I2N, I3N, I4N, I5N, I6N, I7N, I8N, I9N	D18, E18, F18, G18, J18, K18, L18, M18, N18, P18	Inverted phase (–) digital input signal
IORN	B18	In-phase (+) digital input signal additional bit
IOR	B19	Inverted phase (–) digital input signal for additional bit
Clock Inputs		
CLK	H19	In-phase (+) clock input
CLKN	H18	Inverted phase (–) clock input
Digital Outputs		
A0, A1, A2, A3, A4, A5, A6, A7, A8, A9	B16, B15, B14, B13, B12, B11, B10, B9, B8, B7	In-phase (+) digital outputs for port A A0 is the LSB, A9 is the MSB
A0N, A1N, A2N, A3N, A4N, A5N, A6N, A7N, A8N, A9N	A16, A15, A14, A13, A12, A11, A10, A9, A8, A7	Inverted phase (–) digital outputs for port A
AOR/DRAN	B6	In-phase (+) additional bit output for port A or inverted phase (–) output clock in staggered mode for port A
AORN/DRA	A6	Inverted phase (–) additional bit output for port A or in-phase (+) output clock in staggered mode for port A
B0, B1, B2, B3, B4, B5, B6, B7, B8, B9	B5, B4, B3, B2, C2, D2, E2, F2, G2, H2	In-phase (+) digital outputs for port B B0 is the LSB, B9 is the MSB
B0N, B1N, B2N, B3N, B4N, B5N, B6N, B7N, B8N, B9N	A5, A4, A3, A2, B1, C1, D1, E1, F1, G1	Inverted phase (–) digital outputs for port B
BOR/DRBN	J2	In-phase (+) additional bit output for port B or inverted phase (–) output clock in staggered mode for port B

Table 7-1. Pin Description

Symbol	Pin Number	Function
BORN/DRB	H1	Inverted phase (–) additional bit output for port B or in–phase (+) output clock in staggered mode for port B
C0, C1, C2, C3, C4, C5, C6, C7, C8, C9	M2, N2, P2, R2, T2, U2, V1, V2, V3, V4	In-phase (+) digital outputs for port C C0 is the LSB, C9 is the MSB
C0N, C1N, C2N, C3N, C4N, C5N, C6N, C7N, C8N, C9N	L1, M1, N1, P1, R1, T1, U1, W2, W3, W4	Inverted phase (–) digital outputs for port C
COR/DRCN	V5	In-phase (+) additional bit output for port C or inverted phase (–) output clock in staggered mode for port C
CORN/DRC	W5	Inverted phase (–) additional bit output for port C or in-phase (+) output clock in staggered mode for port C
D0, D1, D2, D3, D4, D5, D6, D7, D8, D9	V6, V7, V8, V9, V10, V11, V12, V13, V14, V15	In-phase (+) digital outputs for port D D0 is the LSB, D9 is the MSB
D0N, D1N, D2N, D3N, D4N, D5N, D6N, D7N, D8N, D9N	W6, W7, W8, W9, W10, W11, W12, W13, W14, W15	Inverted phase (–) digital outputs for port D
DOR/DRDN	V16	In-phase (+) additional bit output for port D or inverted phase (–) output clock in staggered mode for port D
DORN/DRD	W16	Inverted phase (–) additional bit output for port D or in-phase (+) output clock in staggered mode for port D
DR	J1	In-phase (+) data ready signal output
DRN	K2	Inverted phase (–) data ready signal output
Additional Functions		
ASYNCRST	B17	Asynchronous reset signal
DRTYPE	K1	Output clock type selection signal
CLKDACTRL	V19	Clock delay cell control signal
RS	L2	Ratio selection signal
SLEEP	A18	Sleep mode enable
STAGG	A17	Staggered output mode selection signal
BIST	V17	Built-in Self Test enable
DIODE	C19	Diode for junction temperature monitoring
NC	D15, D16, R18, R19, T18, T19, V18, W17, W18	No connect pins. (Can be connected to any potential for EV10CS140VTPY)

7.1 EV10CS140 Pinout

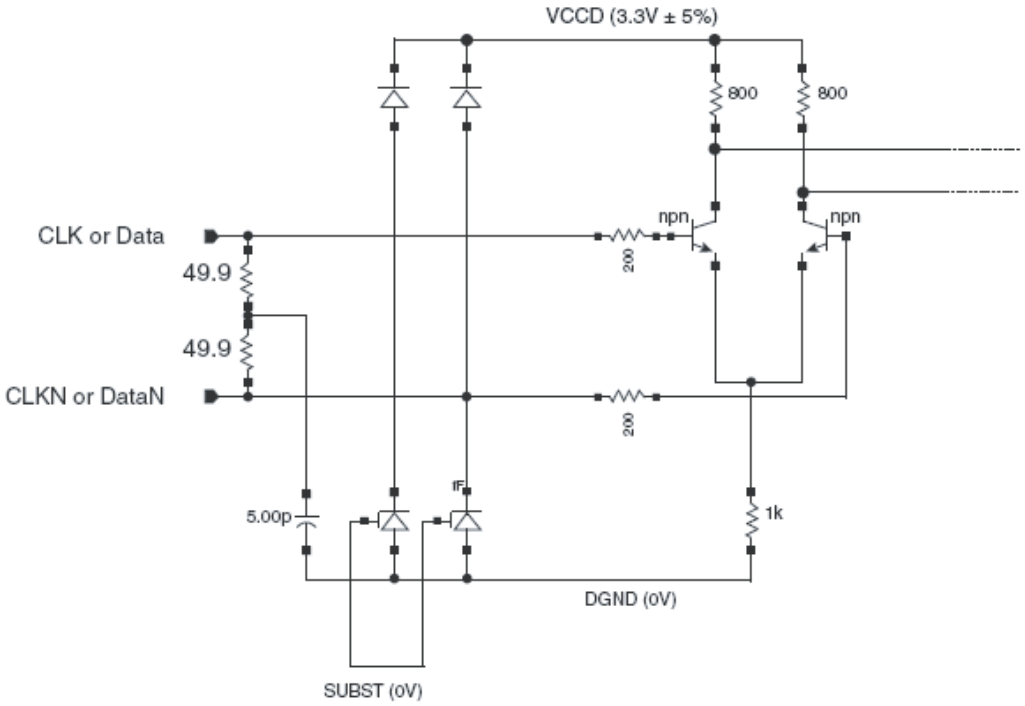
Figure 7-1. EBGA 240 (Bottom View)



8. Input/Output Equivalent Schematics

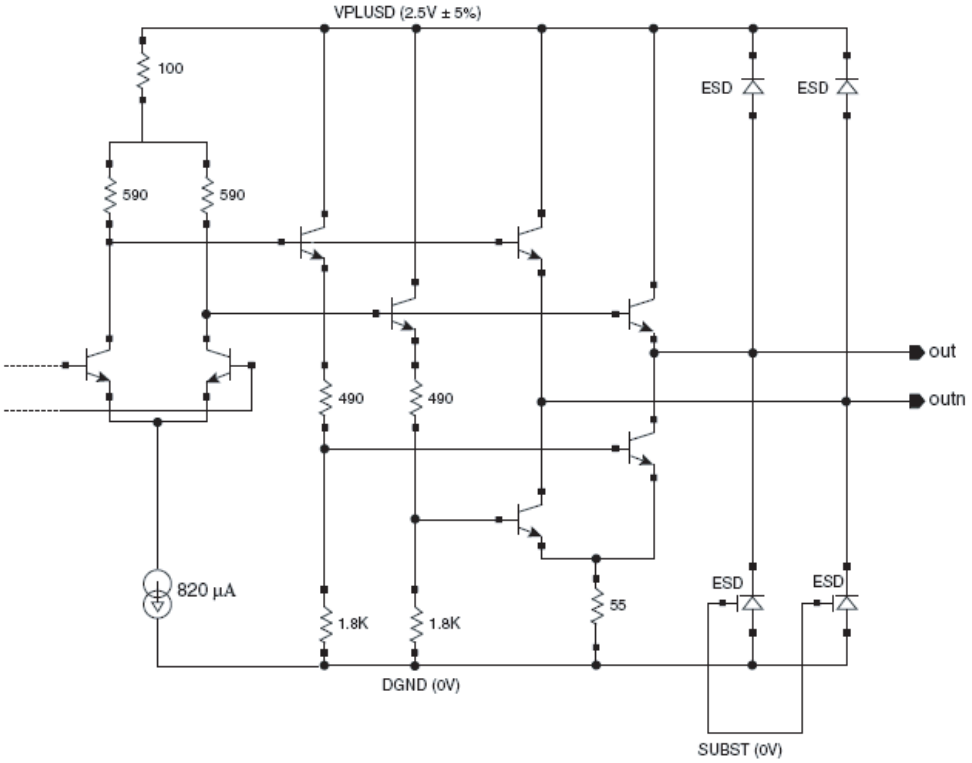
8.1 Data and Clock Differential Input Buffer

Figure 8-1. LVDS Data and LVDS Clock Input Buffer



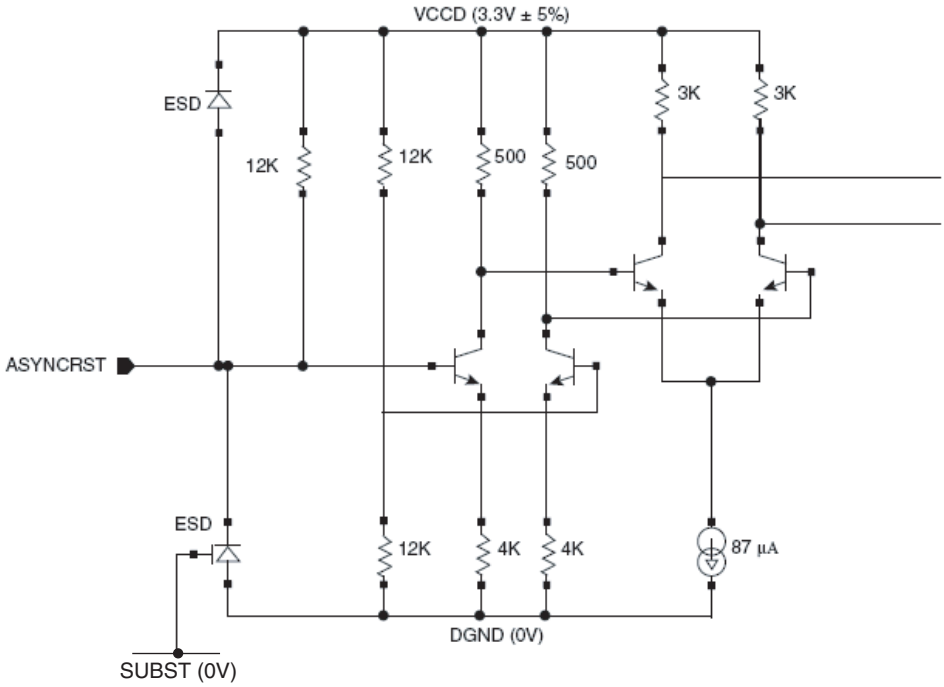
8.2 Data and Clock Output Buffer

Figure 8-2. LVDS Data and Clock Output Buffer



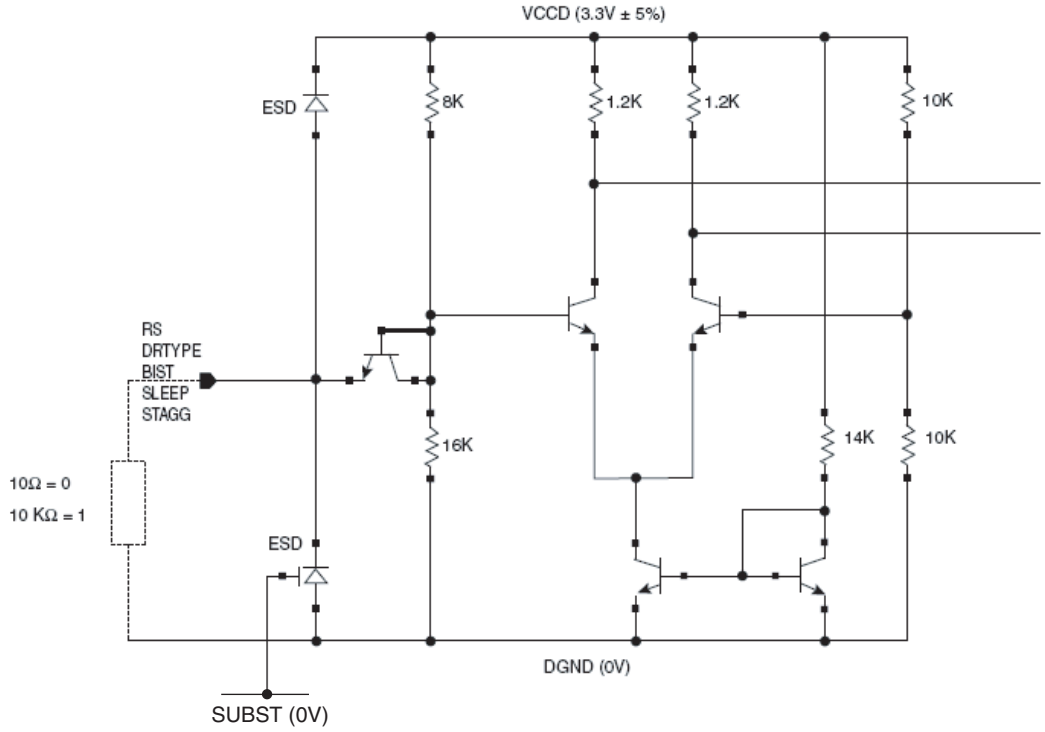
8.3 Asynchronous Reset Buffer

Figure 8-3. Asynchronous Reset Input Buffer



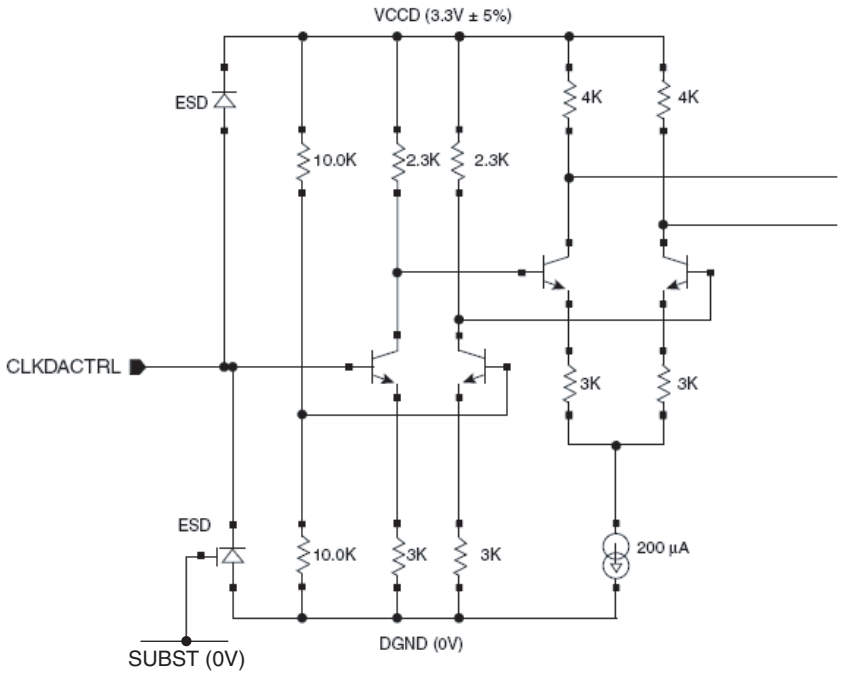
8.4 Control Signal Input Buffers

Figure 8-4. Control Signals Input Buffers: BIST, STAGG, SLEEP, RS, DRTYPE



8.5 CLKDACTRL Delay Cell Control Input Buffer

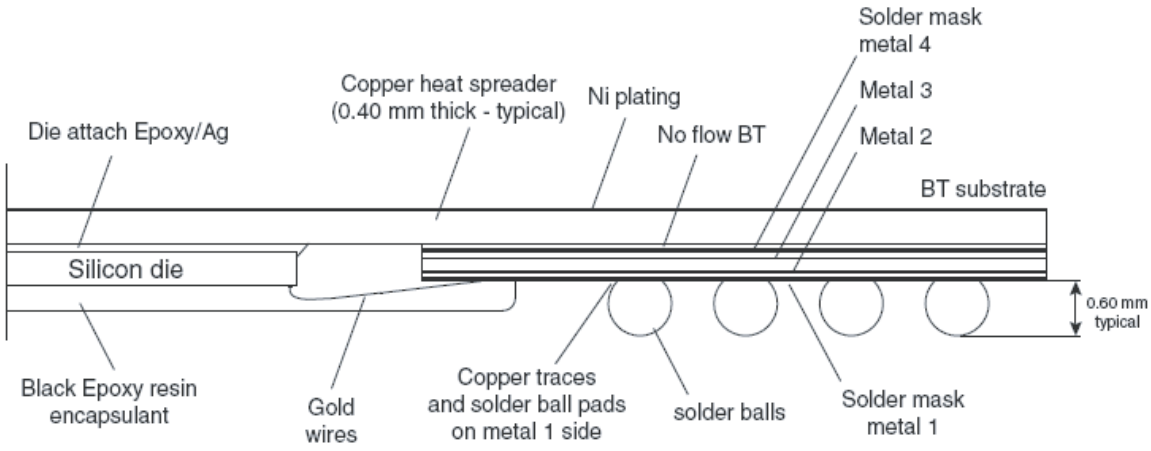
Figure 8-5. CLKDACTRL Delay Cell Control Input Buffer



9. Package Information

9.1 Detailed Cross Section

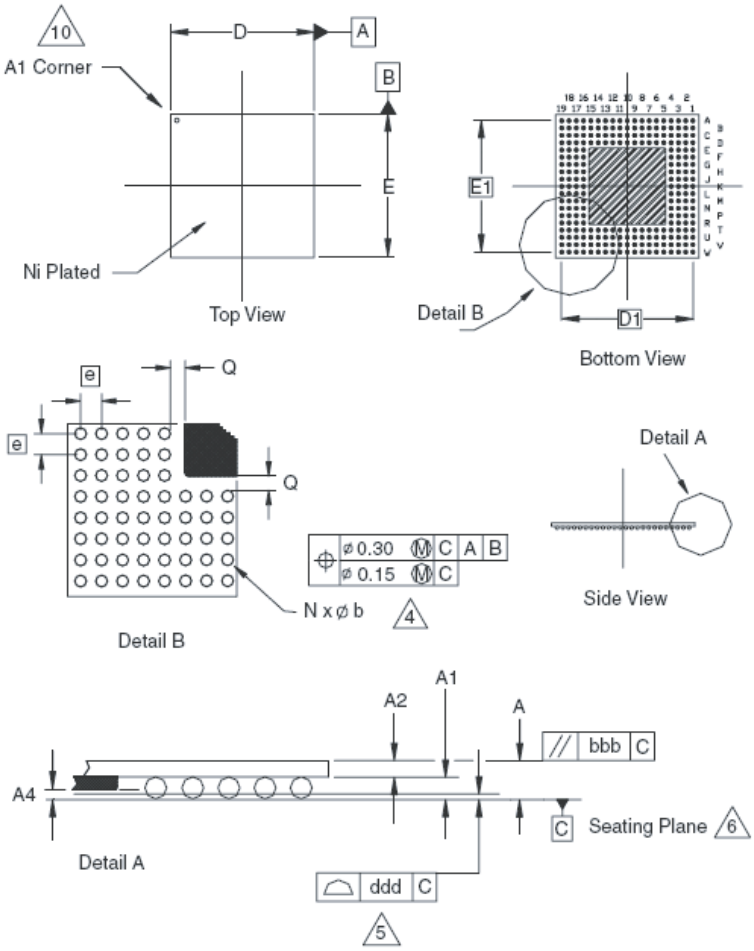
Figure 9-1. Detailed Cross Section of the EBGA 240 Package



Note: In the DMUX package (see above), the die's underside is attached to the copper heat spreader so the copper heat spreader is at GND (0V).
It is recommended to electrically isolate the copper heat spreader from the heat sink if a heat sink is used, in which case adequate low Rth electrical isolation should be used.

9.2 Package Outline

Figure 9-2. EBGA 240 Package Outline



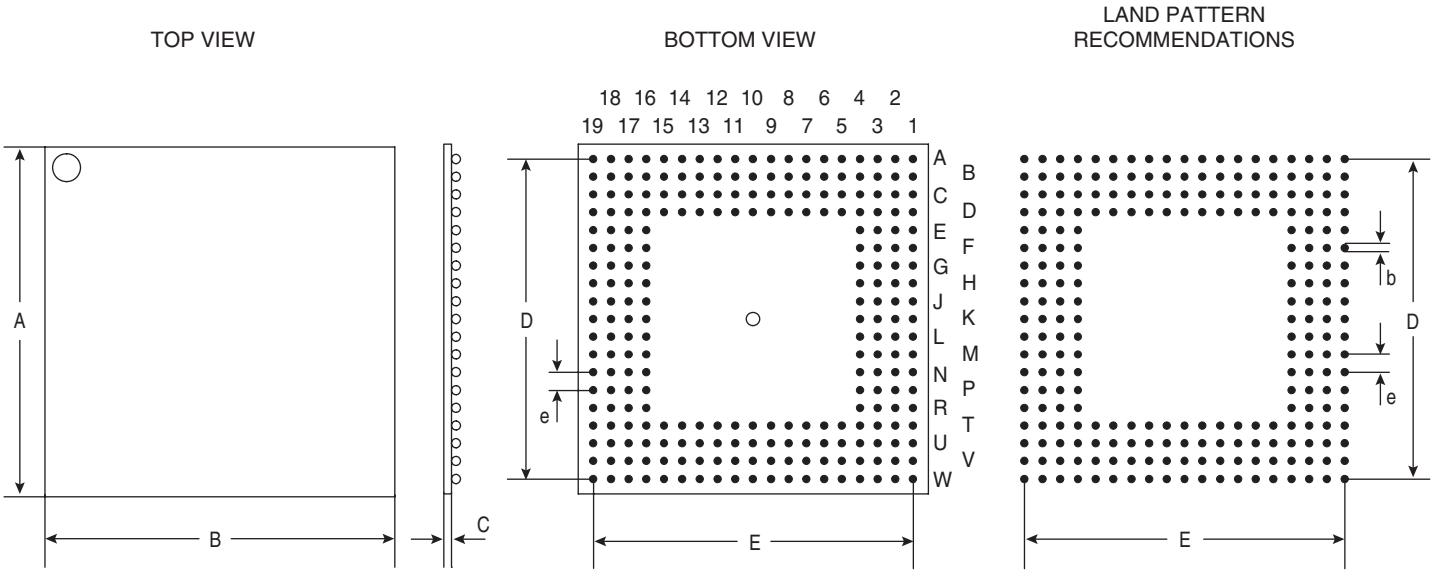
Dimensional References			
Ref	Min	Nom	Max
A	1.25	1.45	1.60
A1	0.50	0.60	0.70
D	24.80	25.00	25.20
D1		22.86 (BSC)	
E	24.80	25.00	25.20
E1		22.86 (BSC)	
b	0.70	0.80	0.90
A2	0.75	0.85	0.95
M		19	
N		240	
bbb			0.25
ddd			0.20
e		1.27 TYP	
A4	0.15		
Q	0.35		
Ref: JEDEC MS-034B Variation BAK-1			

Notes:
1. All dimensions are in millimeters
2. "e" represents the BASIC solder ball grid pitch.
3. "M" represents the BASIC solder ball matrix size, and symbol "N" is the maximum allowable number of balls after depolulating.
4. Dimension "b" is measured at the maximum solder ball diameter parallel to primary Datum C.
5. Dimension "ddd" is measured parallel to primary Datum C.
6. Primary Datum C and seating plane are defined by the spherical crowns of the solder balls.
7. Package surface shall be Ni plated.
8. Encapsulant size may vary with die size.
9. Black spot for pin 1 identification.
10. "A4" is measured at the Edge of encapsulant to the inner Edge of ball pad.
11. Dimensioning and tolerancing per ASME Y14.5 1994.
12. This drawing is for qualification purpose only.

Note: Central area on the bottom side of the package (dashed area) corresponds to dam & fill. (Not a solder paste). This area must not to be soldered to PCB.

9.3 Land Pattern Recommendation

Figure 9-3. EBGA 240 Land Pattern Recommendation

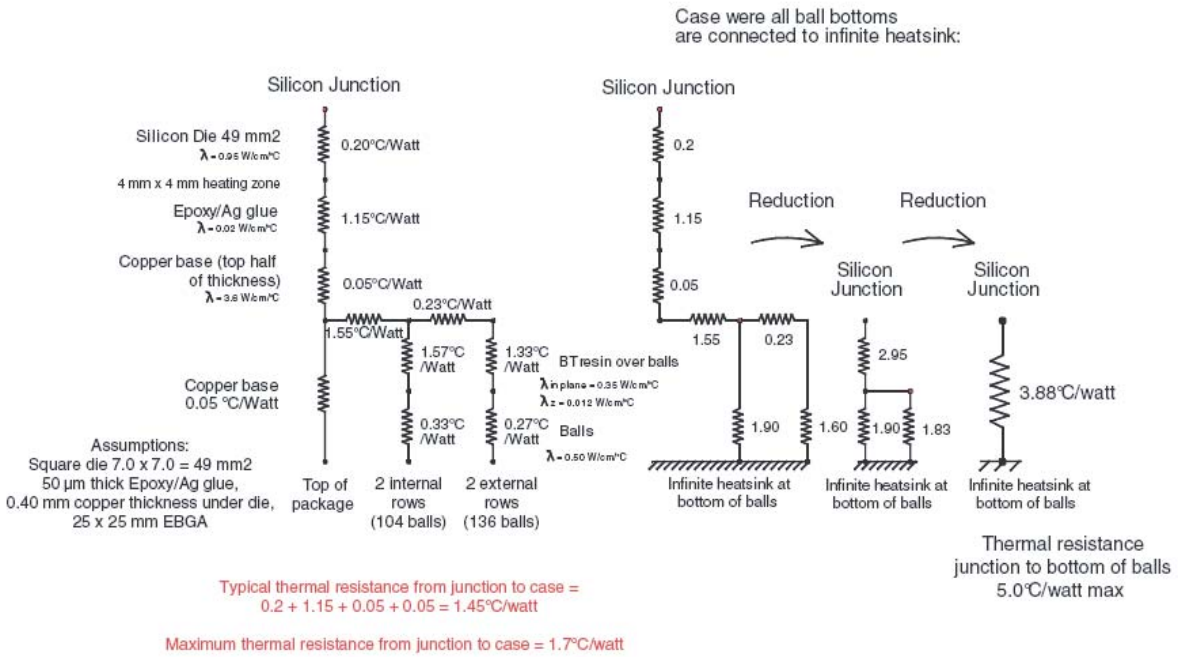


A	B	C	D	E	e	b
25.00	25.00	0.85	22.86	22.86	1.27	0.70

All dimensions are in millimeters

9.4 Thermal and Moisture Characteristics

Figure 9-4. DMUX Thermal Model for EBGA240 (Typical Values) Derived from ANSYS Thermal Simulation



9.5 Moisture Characteristics

This device is sensitive to the moisture (MSL3 according to JEDEC standard). Its shelf life in sealed bag is 12 months at < 40° C and < 90% relative humidity (RH).

Once the bag is opened, devices that will be subjected to infrared reflow, vapor-phase reflow, or equivalent processing (peak package body temp. 260° C) must be:

- mounted within 168 hours at factory conditions of ≤ 30° C/60% RH, or
- stored at ≤ 20% RH

Before mounting, devices will require baking if the humidity indicator is > 20% when read at 23° C ± 5° C.

If baking is required, devices may be baked for:

- 192 hours at 40° C + 5° C/–0° C and < 5% RH for low-temperature device containers, or
- 24 hours at 125° C ± 5° C for high-temperature device containers.

10. Definition of Terms

(TOD)	Digital data Output delay	Delay from the falling edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.
(TDR)	Data ready output delay	Delay from the falling edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output data ready signal (zero crossing) with specified load.
(PD_D)	Pipeline Delay on Data	Number of clock cycles between the data for N being sampled on rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point) and the associated output data for N being made available, (not taking in account the TOD). Total Data propagation delay is PD_D + TOD
(PD_DR)	Clock to Data Ready Delay	Number of clock cycles between rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point) and the Data Ready associated to output data for N being made available, (not taking in account the TDR). Total Data Ready propagation delay is PD_DR + TDR
(TR)	Rise time	Time delay for the output DATA signals to rise from 20% to 80% of delta between low level and high level.
(TF)	Fall time	Time delay for the output DATA signals to fall from 20% to 80% of delta between low level and high level.

11. Ordering Information

Table 11-1. Ordering Information

Part Number	Package	Temperature	Screening	Comments
EV10CS140VTPY	EBGA240 RoHS	Industrial grade $-40°C < T_{amb} < 85°C$	Standard	

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