EV10AS180x-EB Evaluation Board

User Guide

e2v

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Section 1
Introduction

1.1 Scope

The EV10AS180x-EB Evaluation Kit is designed to facilitate the evaluation and characterization of the EV10AS180x 10-bit 1.5 GSps ADC in AC coupled mode.

The EV10AS180x-EB Evaluation Kit includes:

- The 10-bit 1.5 GSps ADC Evaluation board with EV10AS180x ADC soldered on the PCB.
- A CD ROM with the datasheet and device User Guide.

The User Guide describes the use the EV10AS180x-EB Evaluation Kit as an evaluation and demonstration platform and provides guidelines for its proper use.

1.2 Description

The EV10AS180x-EB Evaluation board is very straightforward as it implements e2v EV10AS180x 10-bit 1.5 GSps ADC device, SMA connectors for the sampling clock, analogue inputs and reset input accesses and 2.54 mm pitch connectors compatible with high speed acquisition system probes.

Thanks to its user-friendly interface, the EV10AS180x-EB Kit enables to test all the functions of the EV10AS180x 10-bit 1.5 GSps ADC.

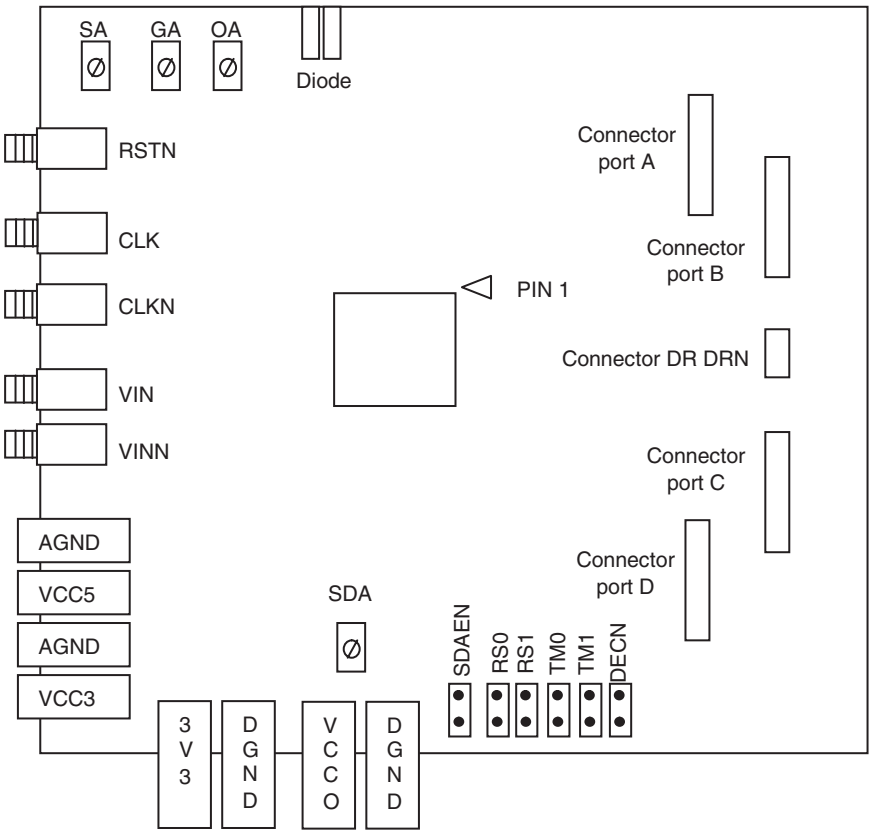
To achieve optimal performance, the EV10AS180x-EB Evaluation board was designed in a 6-metal-layer board using FR4 HTG epoxy dielectric material (200 µm, ISOLA IS410 featuring a resin content of 45%). The board implements the following devices:

- The 10-bit 1.5 Gsps ADC Evaluation board with the EV10AS180x ADC soldered.
- SMA connectors for CLK, CLKN, VIN, VINN, RESETN signals.
- 2.54 mm pitch connectors for the digital outputs, compatible with high speed acquisition system probes.
- Banana jacks (2 mm) for the power supply accesses, the Die junction Temperature monitoring functions.
- Jumpers for SDAEN, RS0, RS1, TM0, TM1, DECN, SDA, SA, OA, GA.
- Potentiometers for SA, OA, GA, SDA.

The board dimensions are 260 mm × 220 mm.

The board comes fully assembled and tested, with the EV10AS180x installed.

Figure 1-1. EV10AS180x-EB Evaluation Board Simplified Schematic



As shown in Figure 1-1 on page 2, different power supplies are required:

- V_{CC5} = 5.2V analogue positive power supply (referenced to AGND).
- V_{CC3} = 3.3V analogue positive power supply (referenced to AGND).
- V_{CCO} = 2.5V digital output power supply (referenced to DGND).
- 3.3V board supply for control functions (referenced to DGND).

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Section 2

Hardware Description

2.1 Board Structure

In order to achieve optimum full speed operation of the EV10AS180x 10-bit 1.5 Gsps ADC, a multi-layer board structure was retained for the evaluation board. Six copper layers are used, dedicated to the signal traces, ground planes and power supply planes.

The board is made in FR4 HTG epoxy dielectric material (ISOLA IS410).

Board characteristics:

- RO4003 for the top and bottom layers, FR4 HTG for the internal layers
- Dielectric thickness: 200 µm
- Dielectric constant: 3.38
- Lands diameter: 750 µm
- GND Via/Land Diameter: 200 µm

The following table gives a detailed description of the board's structure.

Table 2-1. Board Layer Thickness Profile

Layer	Characteristics
Layer 1 Copper layer	Copper thickness = 40 mm (with NiAu finish) AC signals traces = 50Ω microstrip lines DC signals traces
FR4 HTG / dielectric layer	Layer thickness = 200 µm
Layer 2 Copper layer	Copper thickness = 18 µm AGND, DGND (separate planes)
FR4 HTG / dielectric layer	Layer thickness = 349 µm
Layer 3 Copper layer	Copper thickness = 18 µm Power planes = V_{CC5}, V_{CC3}, V_{CCO}
FR4 HTG / dielectric layer	Layer thickness = 350 µm
Layer 4 Copper layer	Copper thickness = 18 µm Power planes = 3V3
FR4 HTG / dielectric layer	Layer thickness = 350 µm

Table 2-1. Board Layer Thickness Profile (Continued)

Layer	Characteristics
Layer 5 Copper layer	Copper thickness = 18 µm AGND, DGND (separate planes)
FR4 HTG / dielectric layer	Layer thickness = 200 µm
Layer 6 Copper layer	Copper thickness = 40 µm (with NiAu finish) AC signals traces = 50Ω microstrip lines DC signals traces

The board is 1.6 mm thick.

The Clock, analogue inputs, reset and ADC functions occupy the top metal layer. The digital data output signals occupy the top and bottom layers.

The Ground planes occupy layer 2 and 5.

Layer 3 and 4 are dedicated to the power supplies.

2.2 Analogue Inputs/Clock Input

The differential clock and analogue inputs are provided by SMA connectors (Reference: JOHNSON 142-0701-851-6).

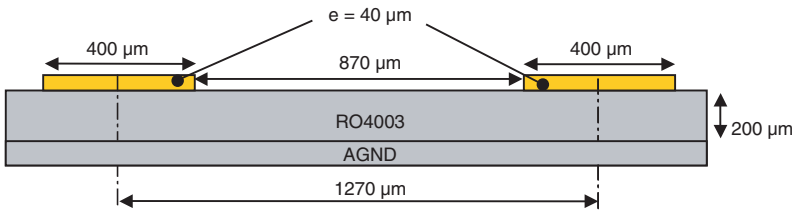
Both pairs are AC coupled using 10 nF capacitors.

Special care was taken for the routing of the analog and clock input signals for optimum performance in the high frequency domain:

- 50Ω lines matched to ±0.1 mm (in length) between VIN and VINN or CLK and CLKN.
- 1270 µm between two differential pairs.
- 400 µm line width.
- 40 µm thickness.
- 870 µm diameter hole in the ground layer below the VIN and VINN or CLK and CLKN ball footprints.
- In addition, the lines for VIN, VINN and CLK, CLKN are matched to one another within ±1mm.
- A clearance in the ground plane below the CLK, CLKN and VIN, VINN package lands is necessary.

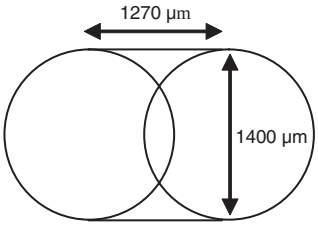
Note: These values have been calculated with RO4003 dielectric material.

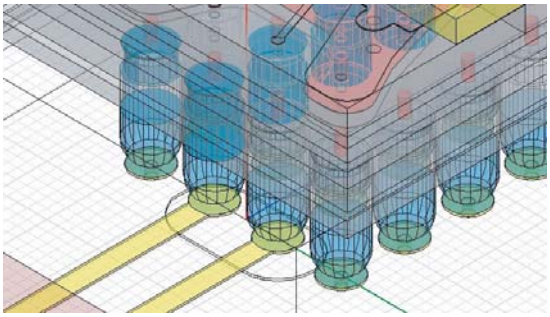
Figure 2-1. Board Layout for the Differential Analog and Clock Inputs with RO4003



Note: The analogue inputs and clock inputs are AC coupled with 10 nF very close to the SMA connectors.

Figure 2-2. Recommended Clearance Under CLK, CLKN, and VIN, VINN on the Ground Plane





2.3 Digital Output Data

The high speed differential output signals (digital output, clock output), are routed in parallel with 50Ω impedance, 370 µm width and a pitch of 0.77 mm.

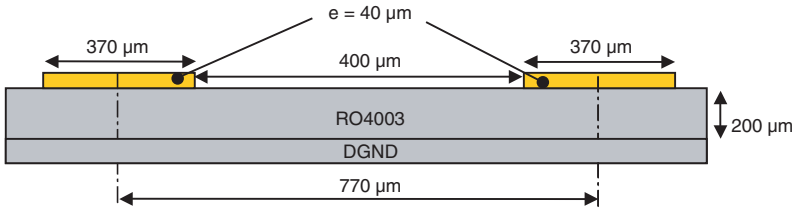
Max difference between any two signals = ±1.5mm.

Max difference between longest and shortest data per port = ±1mm

Max difference between two signals of the same differential pair (Xi, XiN) = ±0.5mm (where X = A, B, C or D, i = 0…9).

Note: These values have been calculated with RO4003 dielectric material.

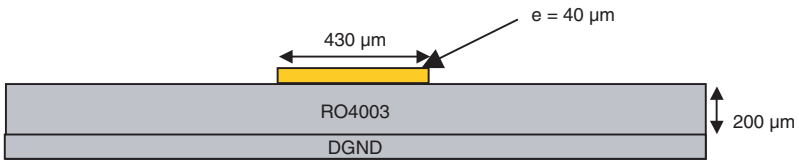
Figure 2-3. Recommended Routing on RO4003 for Digital Output Data Signals



2.4 RSTN

The RSTN signal is a single-ended signal with 50Ω impedance.

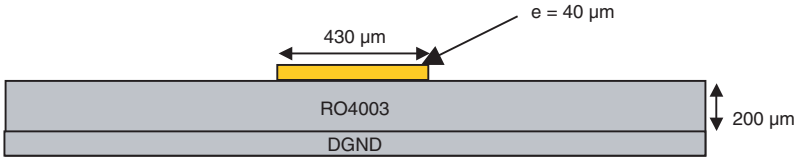
Figure 2-4. Recommended Routing on RO4003 for RSTN Signal



2.5 SA, RSx, TMx, SDA, SDAEN, GA, OA, DECN, Diode

These are "static" signals. They are routed in single-ended 50Ω impedance.

Figure 2-5. Recommended Routing on RO4003 for Static Signal



2.6 Ground Layers

There are 2 separated planes for the AGND and the DGND on the PCB. These planes must be reunited via 0Ω resistors. Only the input clock and analogue input are referenced to AGND, the other parts of the ADC are referenced to DGND.

Important note: AGND and V_{CCO} are not superimposed in order to avoid coupling effects. V_{CC3} and V_{CC5} are referenced to AGND while V_{CCO} is referenced to DGND.

2.7 Power Supplies

Layers 3 and 4 are dedicated to power supply planes:

- V_{CC5}: ADC Analog part supply (V_{CC5} = 5.2V)
- V_{CC3}: ADC Analogue Core and Digital parts supply (V_{CC3} = 3.3V)
- V_{CCO}: ADC Output buffers supply (V_{CCO} = 2.5V)
- 3.3V: external reference for GA, OA, SA and SDA commands.

The supply traces are low impedance and are surrounded by two ground planes (layer 2 and 5).

Each incoming power supply is bypassed at the banana jack by a 1 µF Tantalum capacitor in parallel with a 100 nF chip capacitor.

Each power supply is decoupled as close as possible to the EV10AS180x device by 10 nF in parallel with 100 pF surface mount chip capacitors.

Note: The decoupling capacitors are superimposed with the 100 pF capacitor mounted first.

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Section 3

Operating Characteristics

3.1 Introduction

This section describes a typical configuration for operating the EV10AS180x 10-bit 1.5 Gsps ADC, evaluation board.

The analogue input signals and the sampling clock signal should be accessed in a differential fashion. Band pass filters should also be used to optimize the performance of the ADC both on the analog input and on the clock.

It is necessary to use a very low jitter source for the clock signal (recommended maximum jitter = 225 fs rms).

Note: The analogue inputs and clock are AC coupled on the board.

3.2 Operating Procedure

1. Connect the power supplies and ground accesses through the dedicated banana jacks.
   V_{CC5} = 5.2V, V_{CC3} = 3.3V, V_{CCO} = 2.5V and board supply = 3.3V
2. Connect the clock input signals.
   The clock input level is typically 4 dBm and should not exceed 10 dBm (into 100 differential).
   The clock frequency should be set to 1.5 GHz (for operation in 1:2 or 1:4 DEMUX Ratio).
3. Connect the analogue input signals (the board has been designed to allow only AC coupled analogue inputs).
   Use a low-phase noise High Frequency generator as well as a band pass filter to optimize the analogue input performance.
   The analogue input Full Scale is 500mV peak-to-peak around zero (analogue input providing the Input common mode). It is recommended to use the ADC with an input signal of –12 dBFS max (to avoid saturation of the ADC).
4. Connect the high speed acquisition system probes to the output connectors.
   The digital data are differentially terminated on-board (100Ω) however, they can be probed either in differential.
5. Switch on the ADC power supplies (recommended power up sequence: simultaneous or in the following order: V_{CC3} = 3.3V, V_{CC5} = 5.2V, V_{CCO} = 2.5V and board supply 3.3V).
6. Turn on the RF clock generator.
7. Turn on the RF signal generator.

The EV10AS180x-EB evaluation board is now ready for operation.

Note: An external reset (RSTN) SMA connector or switch is available in case it is necessary to reset the ADC during operation (it is not mandatory to perform an external reset on the ADC for proper operation of the ADC as a power up reset already implemented). This reset is 2.5V CMOS compatible. It is active low (inactive by default on the board).

3.3 Electrical Characteristics

Values in the table below are given for information only, for more accurate values refer to datasheet.

Table 3-1. Recommended Conditions of Use

Parameter	Symbol	Comments	Typ	Unit
Power supplies	V_{CC5}		5.2	V
	V_{CC3}		3.3	V
	V_{CC0}		2.5	V
Differential analog input voltage (Full Scale)	$V_{IN} - V_{INN}$	100Ω differential	500	mVpp
Clock input power level (Ground common mode)	P_{CLK} P_{CLKN}	100Ω differential input	4	dBm

Unless otherwise stated, requirements apply over the full operating temperature range (for performance) and at all power supply conditions.

Table 3-2. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test level
RESOLUTION		10			bit	1,6
ESD CLASSIFICATION		> 1000V (HBM model)			V	NA
POWER REQUIREMENTS						
Power Supply voltage - Analog - Analog Core and Digital - Output buffers	 VCC5 VCC3 VCCO	 5.0 3.15 2.4	 5.2 3.3 2.5	 5.5 3.45 2.6	 V V V	1,6
Power Supply current in 1:1 DEMUX Ratio - Analog - Analog Core and Digital - Output buffers	 I_VCC5 I_VCC3 I_VCCO		 71 300 100	 85 330 110	 mA mA mA	1,6
Power Supply current in 1:2 DEMUX Ratio - Analog - Analog Core and Digital - Output buffers	 I_VCC5 I_VCC3 I_VCCO		 71 312 137	 85 335 160	 mA mA mA	1,6
Power Supply current in 1:4 DEMUX Ratio - Analog - Analog Core and Digital - Output buffers	 I_VCC5 I_VCC3 I_VCCO		 71 325 216	 85 355 240	 mA mA mA	1,6
Power dissipation - 1:1 Ratio with standard LVDS output swing - 1:2 Ratio with standard LVDS output swing - 1:4 Ratio with standard LVDS output swing	 PD PD PD		 1.6 1.75 1.9	 1.9 2.0 2.3	 W W W	1,6

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Table 3-2. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test level
LVDS Data and Data Ready Outputs						
Logic compatibility			LVDS differential			
Output Common Mode(1)	VOCM	1.125	1.25	1.375	V	1,6
Differential output(1)(2)	VODIFF	250	350	450	mVp	1,6
Output level “High”(3)	VOH	1.25	–	–	V	1,6
Output level “Low”(3)	VOL	–	–	1.25	V	1,6
Output data format			Binary			1,6
ANALOG INPUT						
Input type			AC coupled			
Analog Input Common Mode (for DC coupled input)			3.1		V	
Full scale input voltage range (differential mode)	VIN VINN	–125 –125		+125 +125	mVp mVp	1,6
Full scale analog input power level	PIN		–5		dBm	1,6
Analog input capacitance (die only)	CIN		0.3		pF	5
Input leakage current (VIN = VINN = 0V)	IIN		50		µA	5
Analog Input resistance (Differential)	RIN	96	100	104	Ω	1,6
CLOCK INPUT (CLK, CLKN)						
Input type			DC or AC coupled			
Clock Input Common Mode (for DC coupled clock)	VICM		2		V	1,6
Clock Input power level (low phase noise						
sinewave input) at 1.5 GHz	PCLK	0	4	+7	dBm	4
100Ω differential						
Clock input swing (differential voltage) at 1.5 GHz	VCLK VCLKN	±447	±708	±1000	mVp	4
Clock input capacitance (die only)	CCLK		0.3		pF	4
Clock Input resistance (Differential)	RCLK	94	98	102	Ω	4
RSTN (active low)						
Logic compatibility			2.5V CMOS compatible			
Input level “High”	V_{IH}	2.0			V	1,6
Input level “Low”	V_{IL}			0.4	V	1,6
DIGITAL INPUTS (RS0, RS1, DECN, SDAEN, TM1, TM0)						
Logic low - Resistor to ground - Voltage level - Input current	 R_{IL} V_{IL} I_{IL}	 0 – –		 10 0.5 450	 Ω V µA	1,6
Logic high - Resistor to ground - Voltage level - Input current	 R_{IH} V_{IH} I_{IH}	 10k 2.0 –		 infinite – 150	 Ω V µA	1,6
OFFSET, GAIN & SAMPLING DELAY ADJUST SETTINGS (OA, GA, SDA)						
Min voltage for minimum Gain, Offset or SDA	Analog_min	2*Vcc3/3 – 0.5			V	1,6

Table 3-2. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test level
Max voltage for maximum Gain, Offset or SDA	Analog_max			2*Vcc3/3 + 0.5	V	1,6
Input current for min setting	I_{min}			200	µA	1,6
Input current for nominal setting	I_{nom}			50	µA	1,6
Input current for max setting	I_{max}			200	µA	1,6
ANALOG SETTINGS (SA)						
SA voltage for default swing value	Smax			2*Vcc3/3		1,6
SA voltage for minimum swing value	S_{min}	2*Vcc3/3 – 0.5				1,6
Input current (low, for default swing value	I_{min}			50	µA	1,6
Input current (high) for min swing value	I_{max}			150	µA	1,6

Notes: 1. Assuming 100Ω termination ASIC load.
2. VODIFF can be lowered down to 100 mV with SA pin to reduce power consumption.
3. V_{OH} min and V_{OL} max can never be 1.25V at the same time when VODIFFmin.

Section 4

Application Information

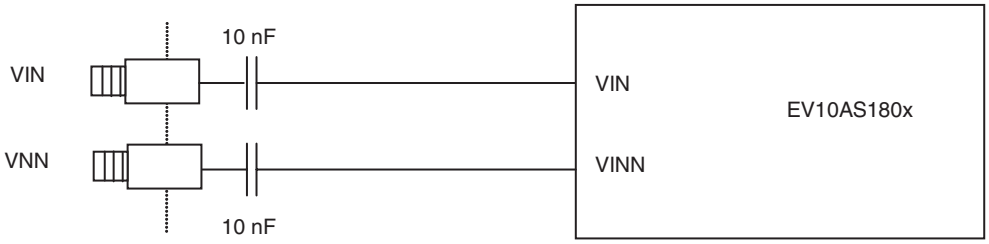
4.1 Analogue Input

The analogue input (VIN, VINN) are entered in differential AC coupled mode as described in Figure 4-1.

It is recommended to use a differential source to drive the analogue inputs of this ADC (external balun or differential amplifier). Please refer to Section Test Bench Description for more information.

In order to optimize the performance of the ADC, it is also recommended to use a band pass filter on the analogue input path.

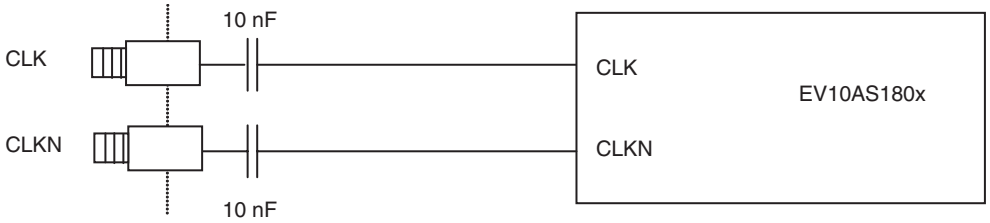
Figure 4-1. Differential Analogue Inputs Implementation



4.2 Clock Input

It is recommended to use a differential source to drive the clock input. The clock is AC coupled via 10 nF capacitors as described in Figure 4-2. Please refer to Section Test Bench Description for more information.

Figure 4-2. Clock Input Implementation



The jitter performance on the clock is crucial to obtain optimum performance from the ADC. We thus recommend to use a very low phase noise clock and to filter the clock signal if a fixed frequency is used.

4.3 RESETN input

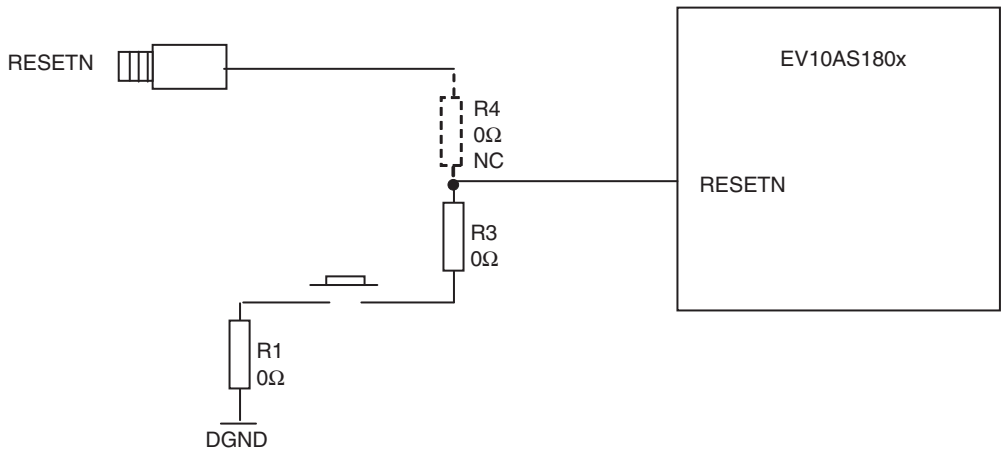
The RESETN signal can be applied by using a switch (SW5):

- By default, RESETN is floating, it is not active, the ADC is in normal mode;
- When the switch is activated, it connects RESETN to ground, which performs a reset on the ADC (reset of the clock circuitry, after reset, the first data will be seen on port A).

It is also possible to apply a signal via the SMA connector, providing R4 is connected (0 ohm) and R3 is removed.

The reset signal is implemented as illustrated in Figure 4-3.

Figure 4-3. RESETN Input Implementation



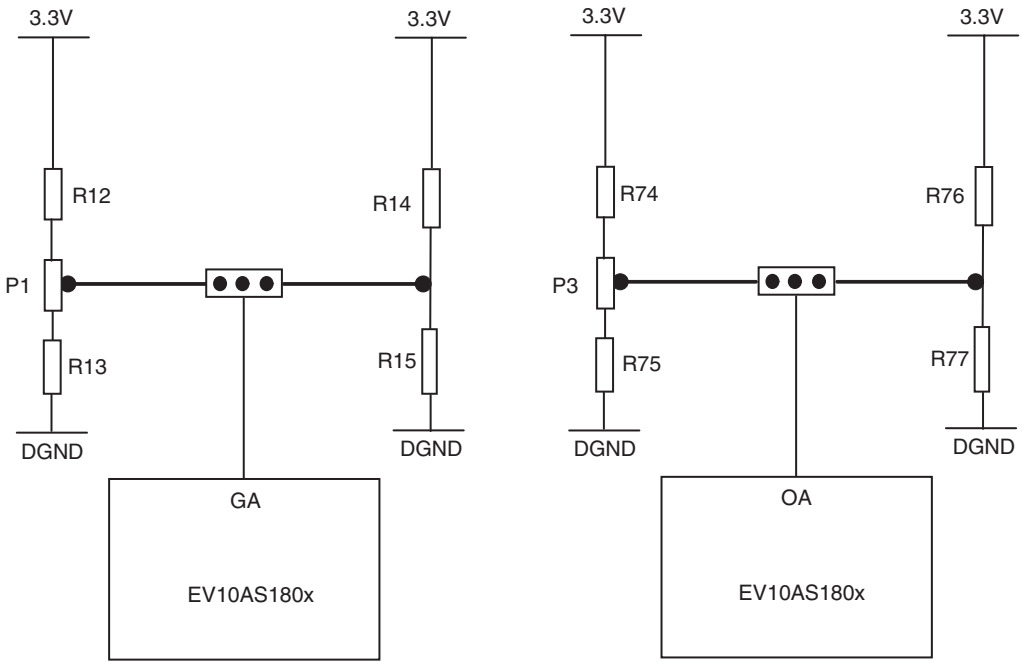
4.4 SA, GA, OA, SDA and SDAEN Commands

4.4.1 GA and OA Commands

These signals are connected by default via their respective jumper to the command middle value (ie. $2 \times V_{CC3}/3 = 2.2V$).

When the jumper is removed, it is possible to tune the OA and GA commands between $(2 \times V_{CC3}/3 - 0.5V)$ to $(2 \times V_{CC3}/3 + 0.5V)$.

Figure 4-4. GA and OA Commands Implementation



With:

R12 = R74 = 240Ω

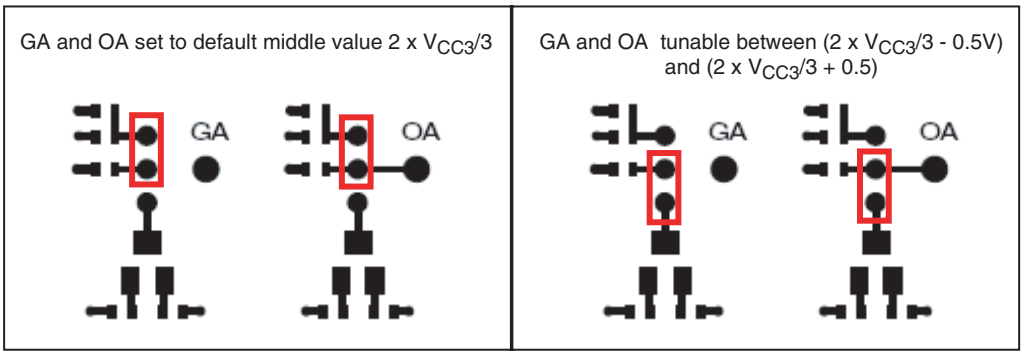
R14 = R76 = 649Ω

P1 = P3 = 1K

R13 = R75 = 1.05 kΩ

R15 = R77 = 1.33 kΩ

Figure 4-5. GA and OA Commands Jumper Settings

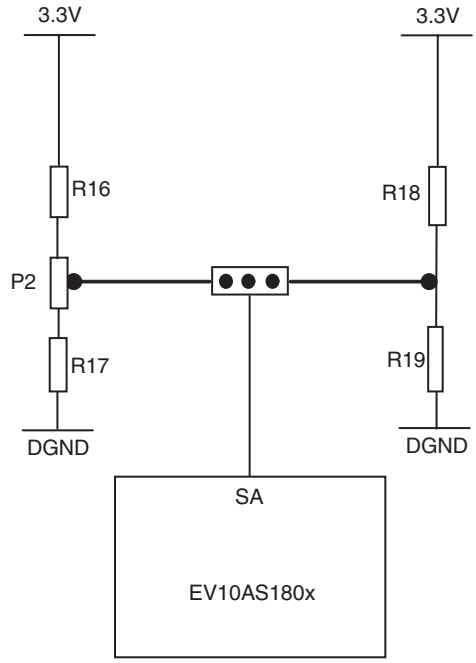


4.4.2 SA Command

This signal is connected by default via its jumper to the command middle value (ie. 2 × V_{CC3}/3 = 2.2V).

When the jumper is removed, it is possible to tune the OA and GA commands between (2 × V_{CC3}/3 – 0.5V) to (2 × V_{CC3}/3 + 0.5V).

Figure 4-6. SA Command Implementation



With:

R16 = 1 kΩ

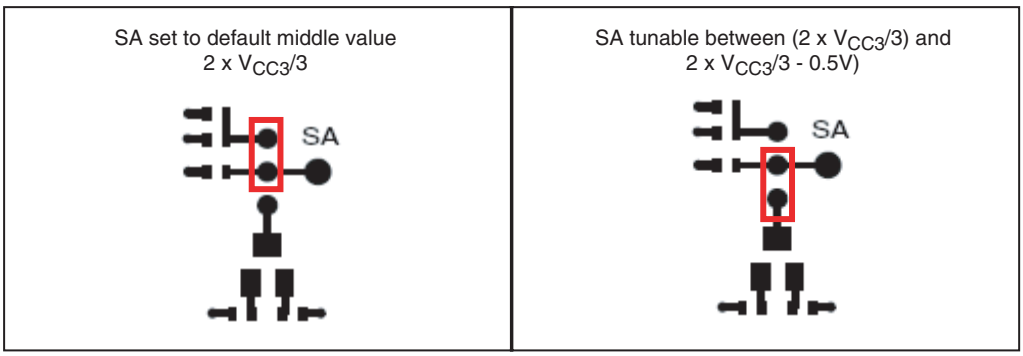
R18 = 649Ω

P2 = 1K

R17 = 1.62 kΩ

R19 = 1.33 kΩ

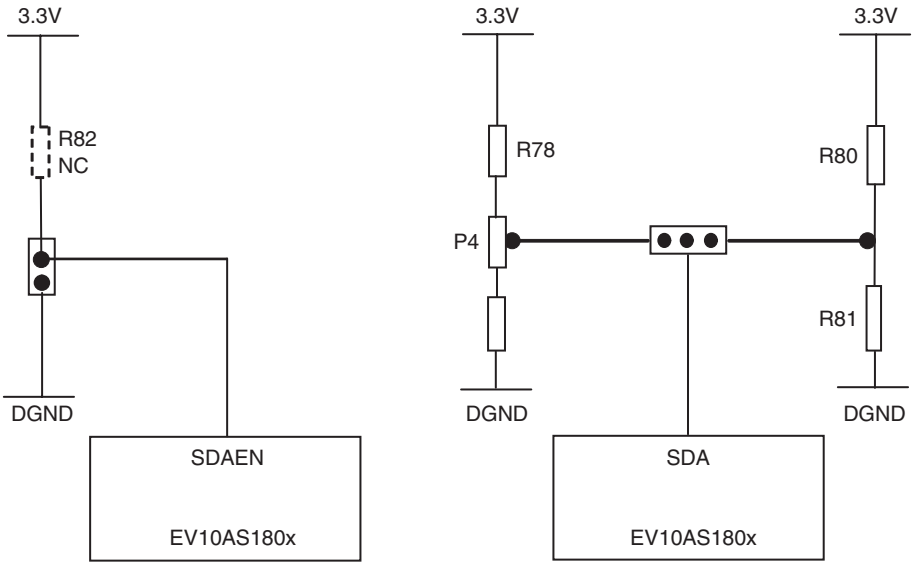
Figure 4-7. SA Command Jumper Settings



4.4.3 SDAEN and SDA Commands

SDAEN signal allows to activate the SDA command when its jumper is OUT or connected as described in Figure 4-9 on page 5. When the SDA function is activated via SDAEN, then it is possible to tune the sampling delay of the ADC by tuning the SDA command between ($2 \times V_{CC3}/3 - 0.5V$) and ($2 \times V_{CC3}/3 + 0.5V$) by ±40 ps around the nominal Aperture delay of the ADC.

Figure 4-8. SDAEN and SDA Commands Implementation



With:

R82 = 10 kΩ (NC: can be connected to provide a true High level to SDAEN)

R78 = 240Ω

R80 = 649Ω

P4 = 1K

R79 = 1.05 kΩ

R81 = 1.33 kΩ

Figure 4-9. SDAEN Command Jumper Settings

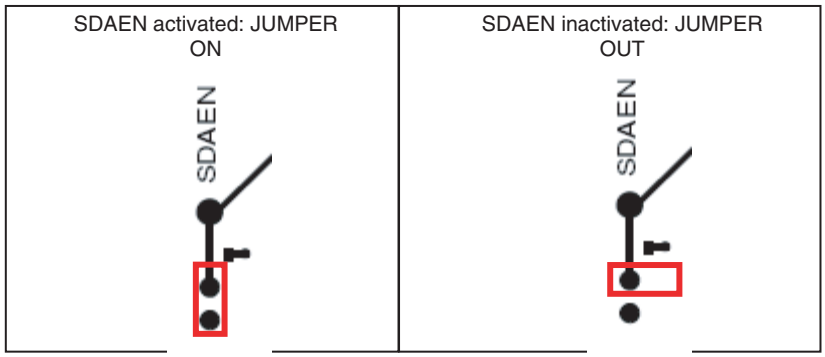
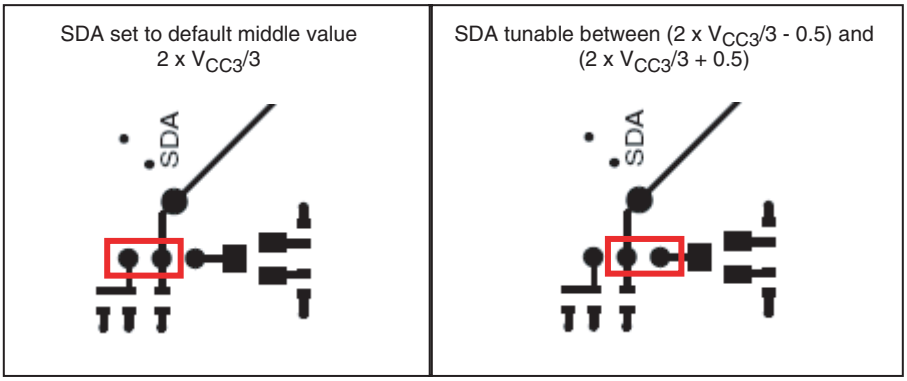


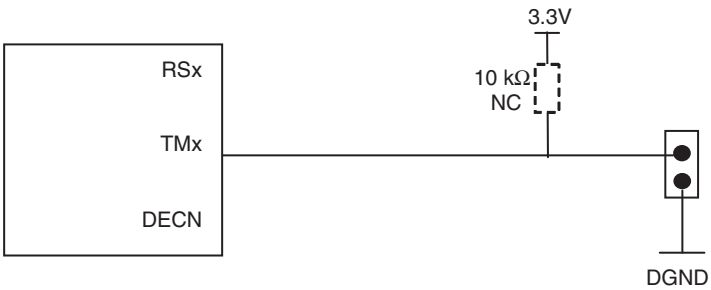
Figure 4-10. SDA Command Jumper Settings



4.5 RSx, TMx and DECN Commands

The RSx, TMx and DECN functions are implemented on board with a jumper which can be ON or OUT (default setting is when the Jumpers are OUT, refer to Figure 4-12 on page 7). A 10 kΩ resistor can be connected in case a pull up is necessary to force a high level on these signals. This resistor is not connected.

Figure 4-11. RSx, TMx and DECN Commands Implementation



The default setting for RSx, TMx and DECN is when their respective jumper is OUT (refer to Figure 4-12). This gives a default setting of the ADC as described below (refer also to Table 4-1):

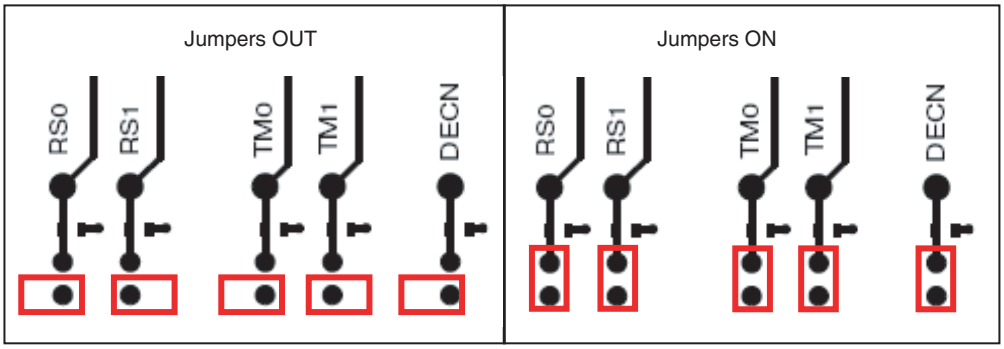
- RS1 = RS0 = Logic High = Jumper OUT -> 1:2 DMUX mode
- TM1 = TM0 = Logic High = Jumper OUT -> Test mode inactive
- DECN = Logic High = Jumper OUT -> Decimation Mode inactive

When the jumper are on (refer to Figure 4-12), the different settings are described in Table 4-1.

Table 4-1. RSx, TMx and DECN Commands Jumper Position

Function	Logic Level	Jumper position	Description
DECN	0	ON	Decimation by 8
	1	OUT	Normal conversion (no decimation)
RS<1:0>	01	RS1 : ON RS0 : OUT	1:1 DEMUX Ratio (Port A)
	11	RS1 : OUT RS0 : OUT	1:2 DEMUX Ratio (Ports A and B)
	10	RS1 : OUT RS0 : ON	1:4 DEMUX Ratio (Ports A, B C and D)
	00	RS1 : ON RS0 : ON	Not used
TM<1:0>	01	TM1 : ON TM 0 : OUT	Static Test (all “0”s at the output for VOL test)
	11	TM 1 : OUT TM 0 : OUT	Normal conversion mode (default mode)
	10	TM 1 : OUT TM 0 : ON	Static Test (all “1”s at the output for VOH test)
	00	TM1 : ON TM0 : ON	Dynamic test (checker board pattern = all bits toggling from “0” to “1” or “1” to “0” every cycle with 1010101010 or 0101010101 patterns)

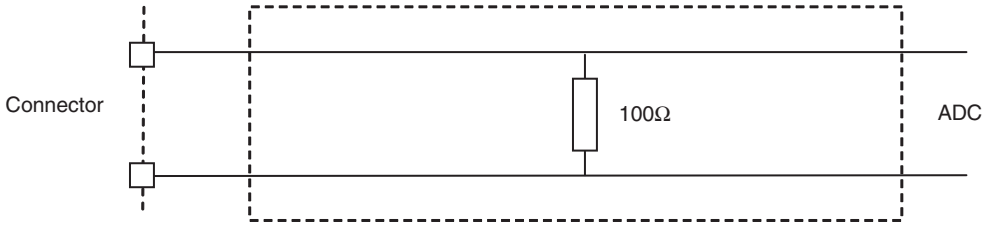
Figure 4-12. RSx, TMx, DECN Command Jumper Settings



4.6 Output Data

The digital outputs are compatible with LVDS standard. They are on-board 100Ω differentially terminated as described in Figure 4-13.

Figure 4-13. Differential Digital Outputs Implementation



Double row 2.54 mm pitch connectors are used for the digital output data. The upper row is connected to the signal while the lower row is connected to Ground, as illustrated in Figure 4-5 on page 3 and Figure 4-6 on page 4. The connectors are vertical connectors.

Figure 4-14. Differential Digital Outputs 2.54 mm Pitch Connector (X = A, B)

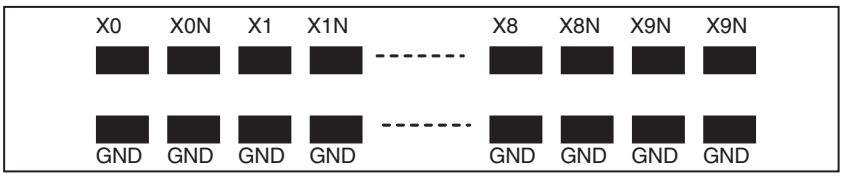


Figure 4-15. Differential Digital Outputs 2.54 mm Pitch Connector (Port A)

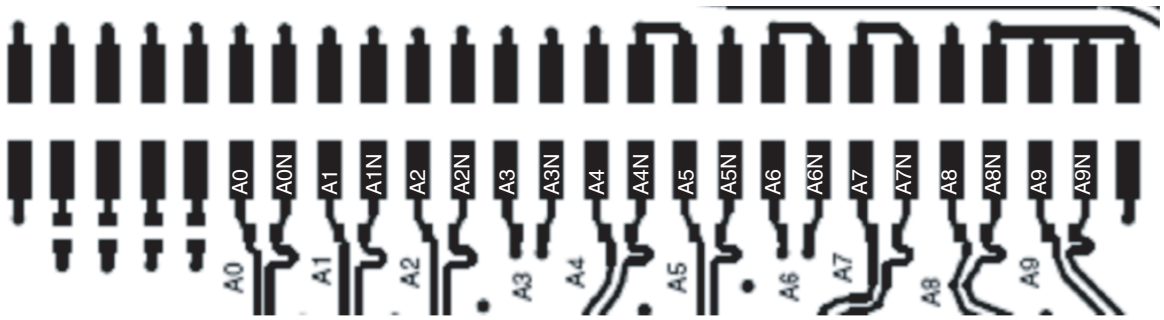


Figure 4-16. Differential Digital Outputs 2.54 mm Pitch Connector (Port B)

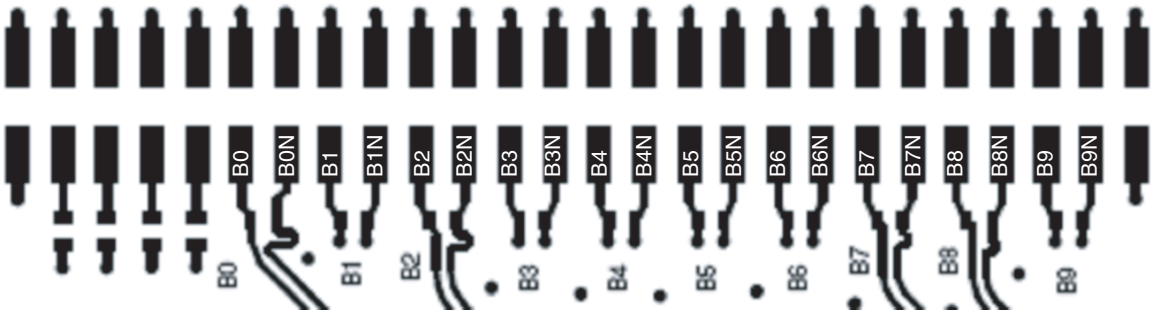


Figure 4-17. Differential Digital Outputs 2.54 mm Pitch Connector (X = C, D)

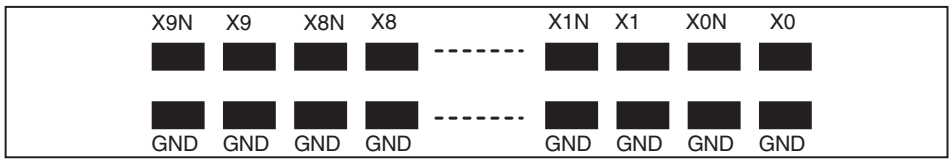


Figure 4-18. Differential Digital Outputs 2.54 mm Pitch Connector (Port C)

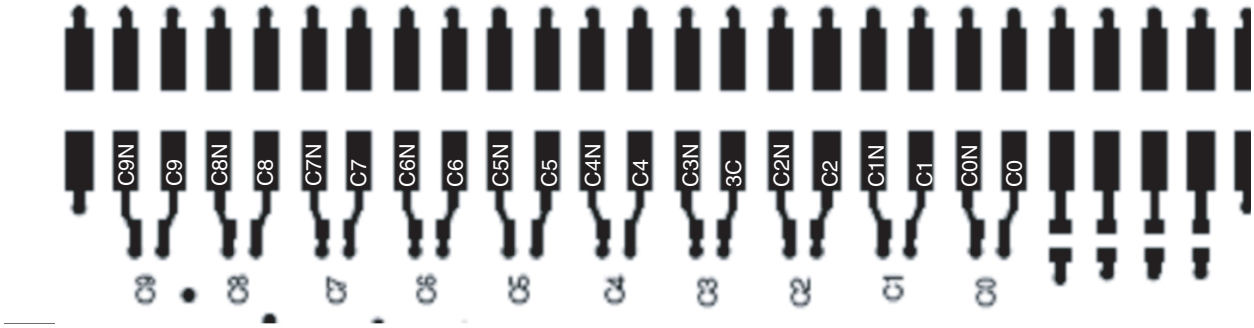


Figure 4-19. Differential Digital Outputs 2.54 mm Pitch Connector (Port D)

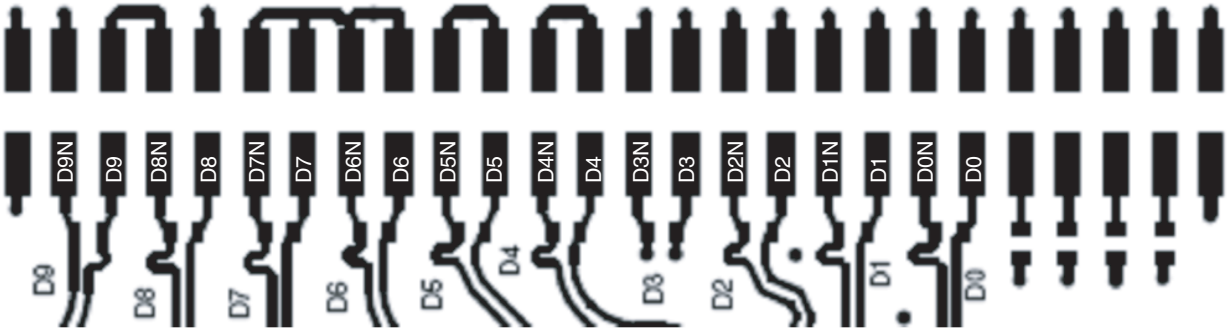
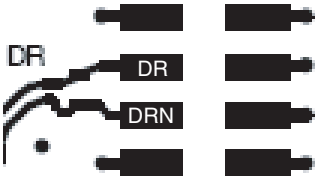


Figure 4-20. Differential Digital Outputs 2.54 mm Pitch Connector (DR, DRN Signal)



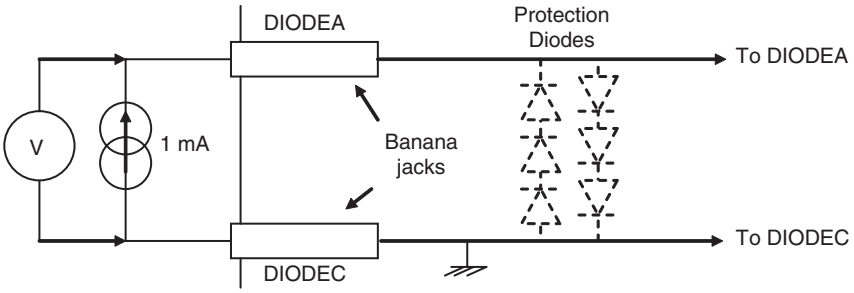
The data are output in Binary format and in double data rate (the output clock frequency is half the data rate and thus half the input clock frequency in 1:1 DMUX mode, or ¼ the input clock frequency in 1:2 DMUX mode and 1/8 the input clock frequency in DMUX 1:4 mode).

4.7 Diode for Junction Temperature Monitoring

Two 2 mm banana jacks are provided for the die junction temperature monitoring of the ADC.

One banana jack is labeled DIODEA and should be applied a current of up to 1 mA (via a multimeter used in current source mode) and the second one is connected to DIODEC.

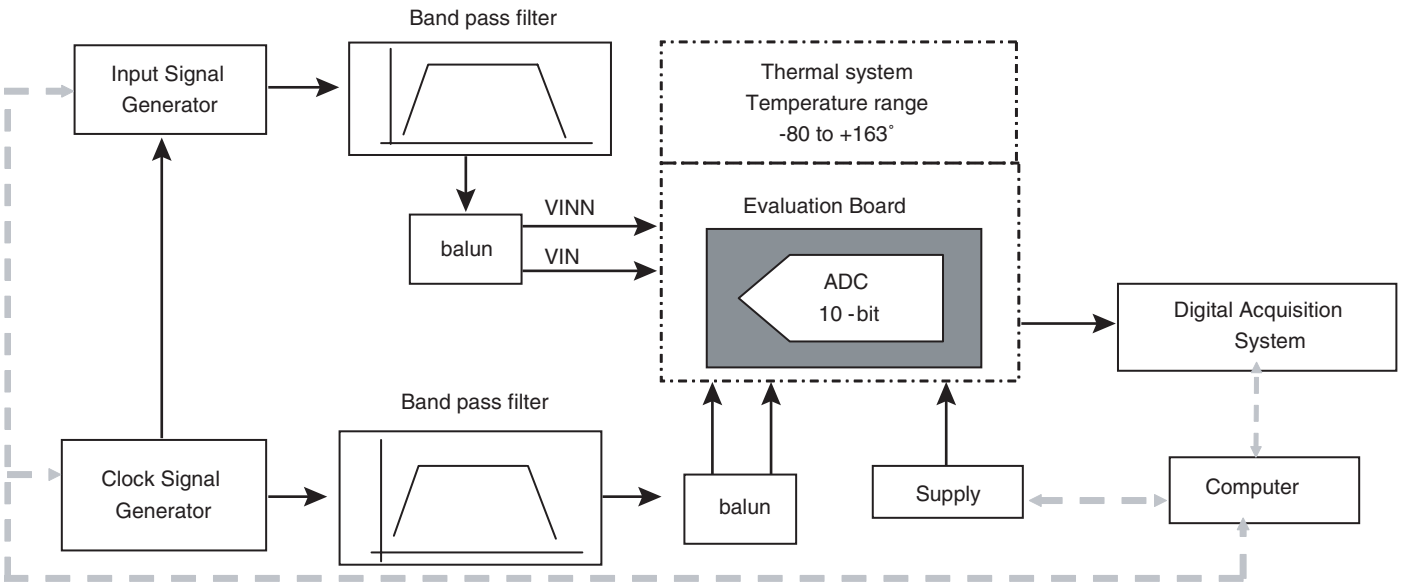
Figure 4-21. Die Temperature Monitoring Test Setup



Note: The protection diodes are NC.

4.8 Test Bench Description

Figure 4-22. Test Bench Description



- Equipment (for example)
  - Input Signal Generator: Agilent E4426B
  - Clock Signal Generator: Agilent E4426B
  - Power Supply: Agilent 6629A
  - Logic Analyser: HP16500C
  - Balun: MACOM-H9 (2MHz => 2GHz)
  - Band pass filter: LORCH (500MHz => 1GHz) & LORCH (1GHz => 2GHz)

Section 5

Ordering Information

5.1 Ordering Information

Table 5-1. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
EV10AS180AGS-EB	CI-CGA255	Ambient	Prototype	Evaluation board

Section 6

Appendix

6.1 EV10AS180x-EB Electrical Schematics

Figure 6-1. Power Supplies Bypassing

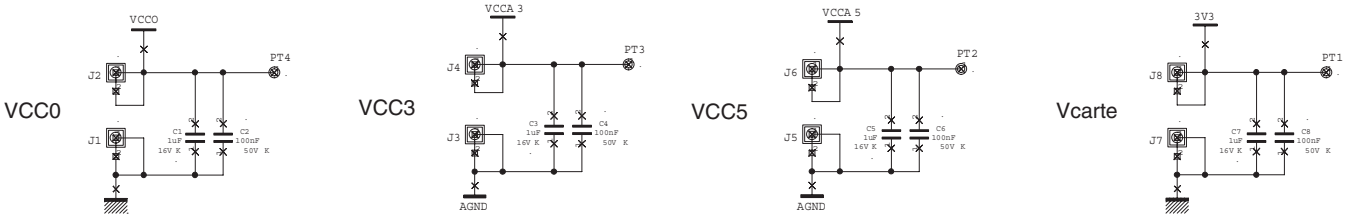


Figure 6-2. Power Supplies Decoupling

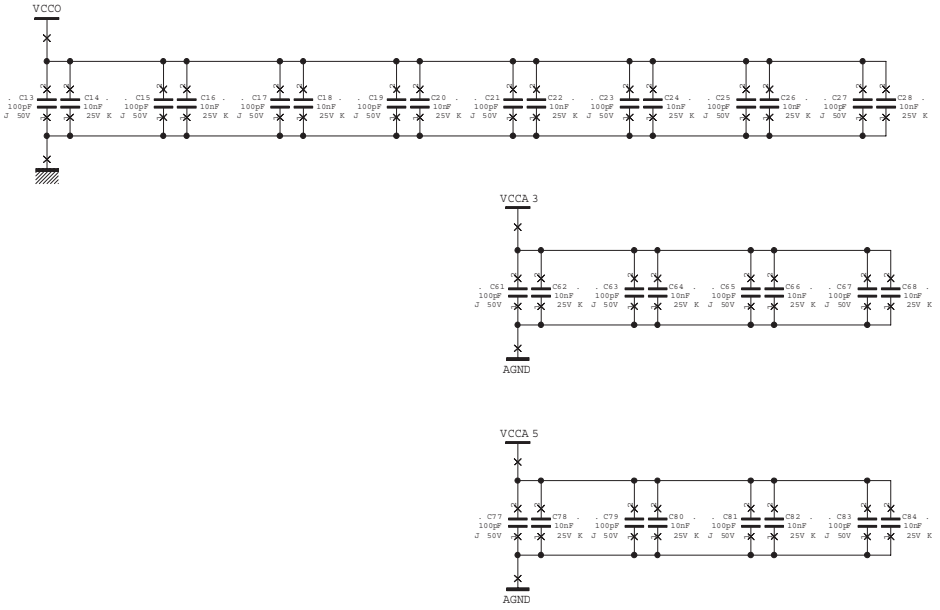


Figure 6-3. Electrical Schematics

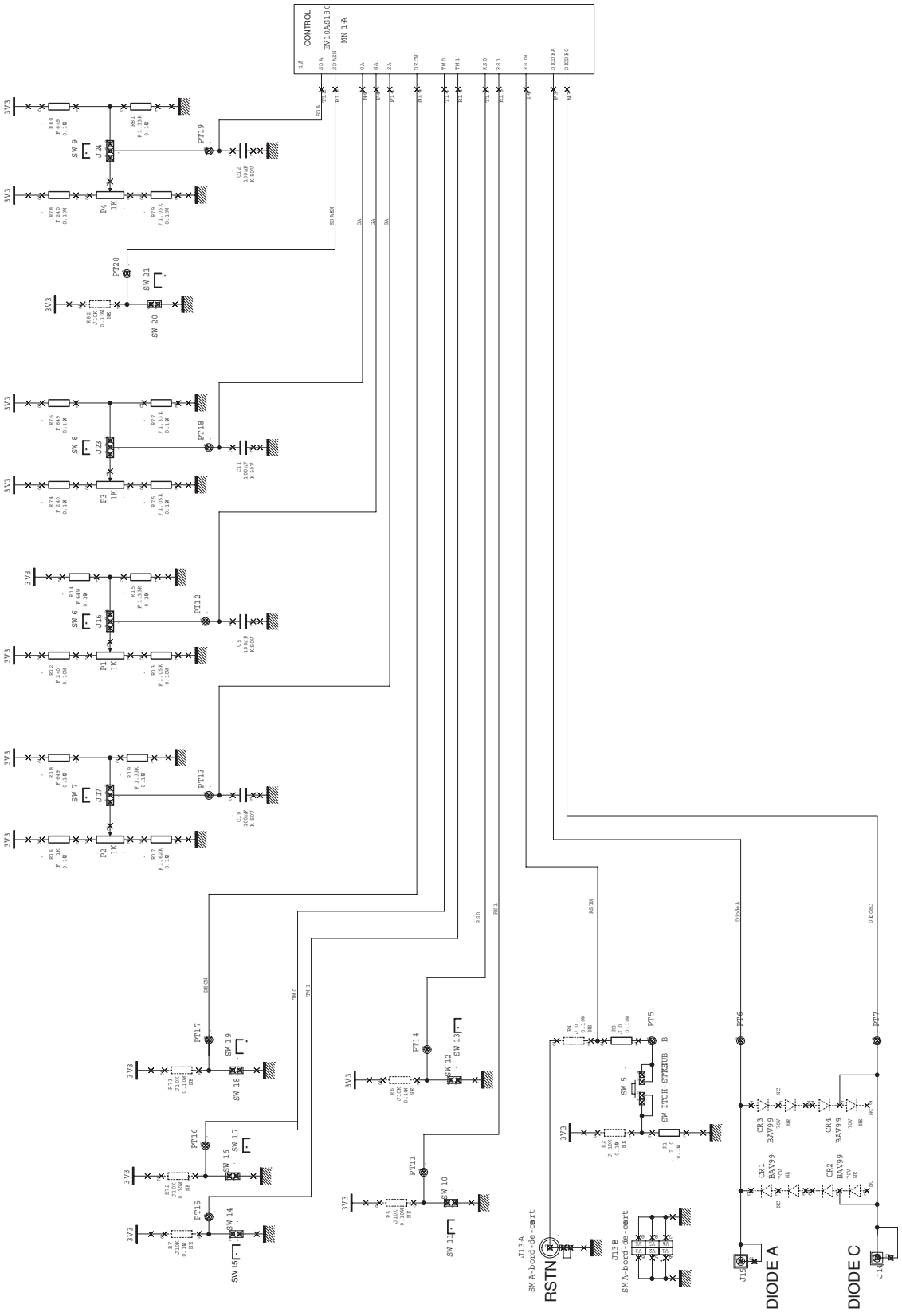


Figure 6-4. Electrical Schematics (Analogue and Clock Input)

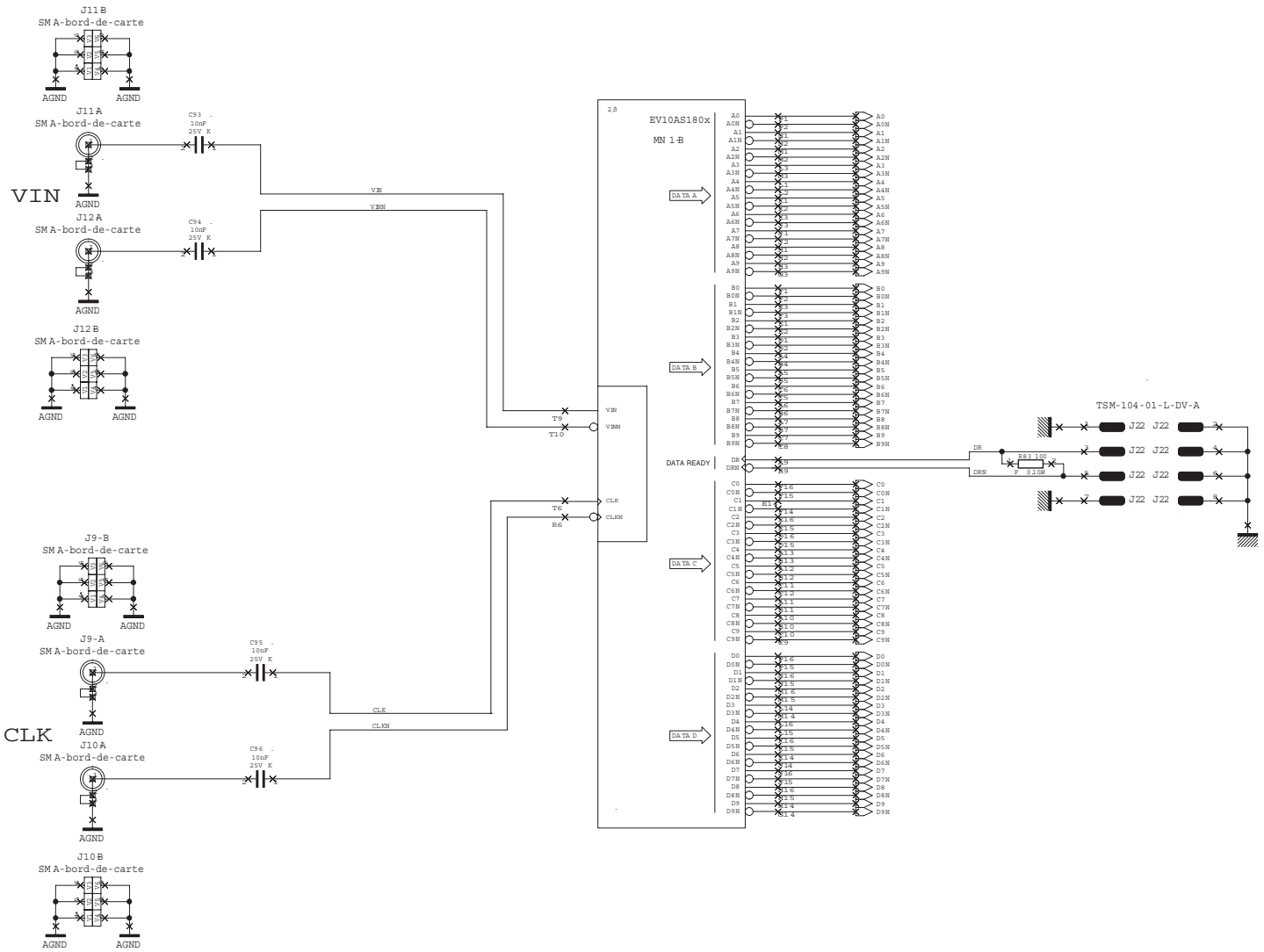
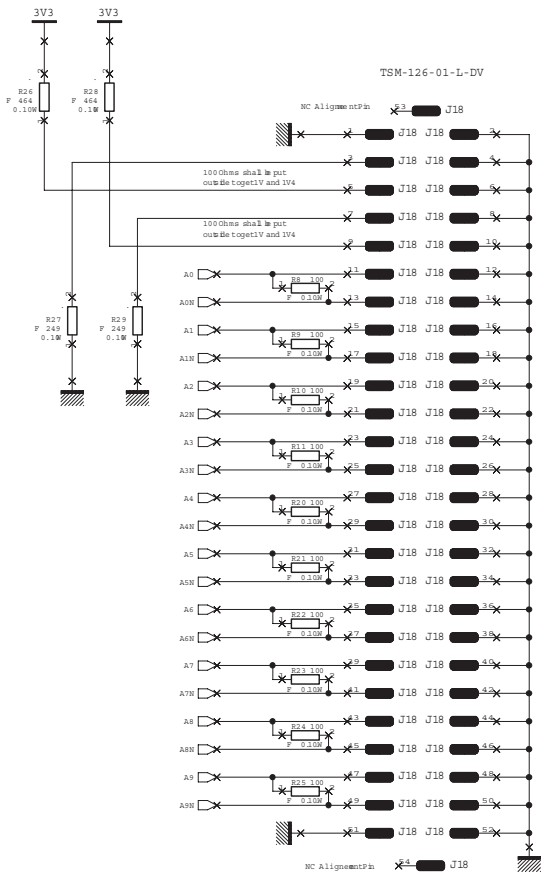
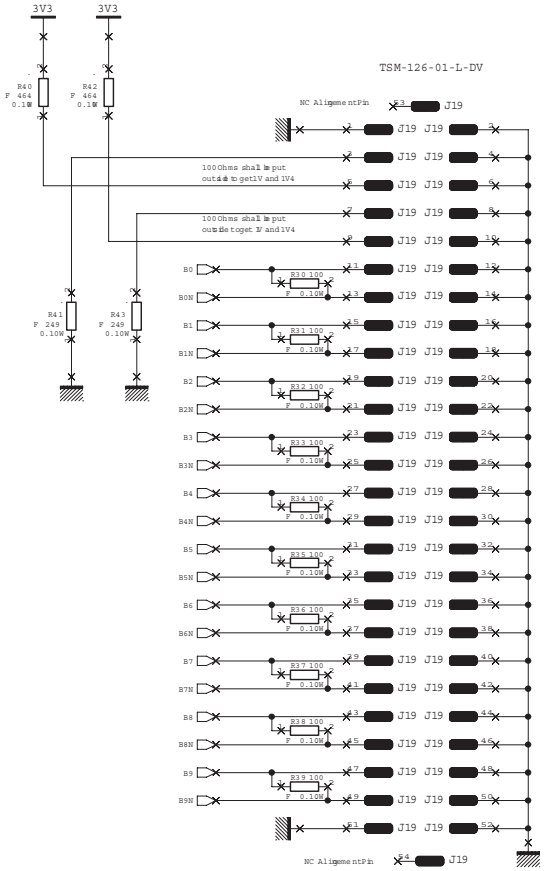


Figure 6-5. Electrical Schematics (Output Connectors Ports A and B)

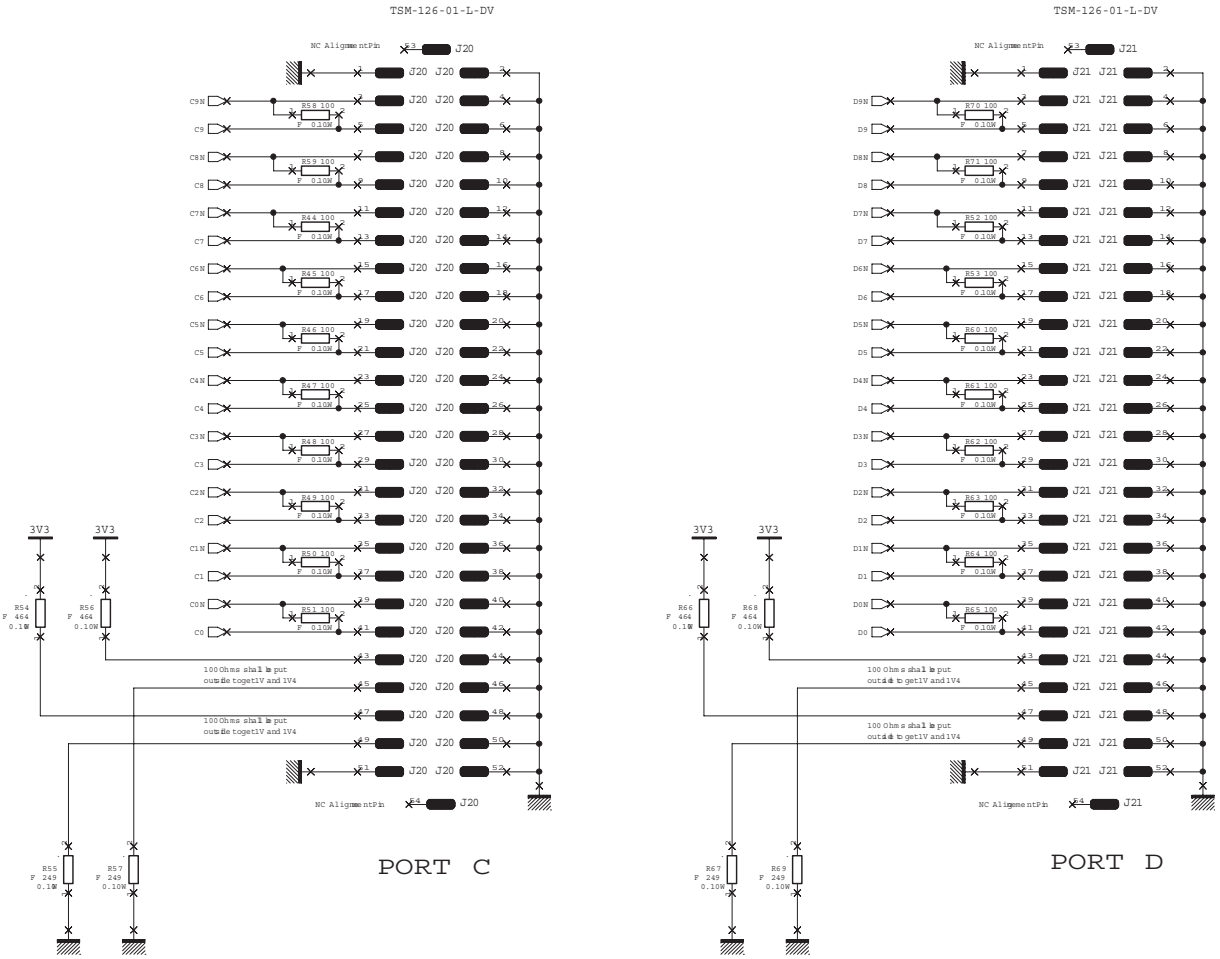


PORT A



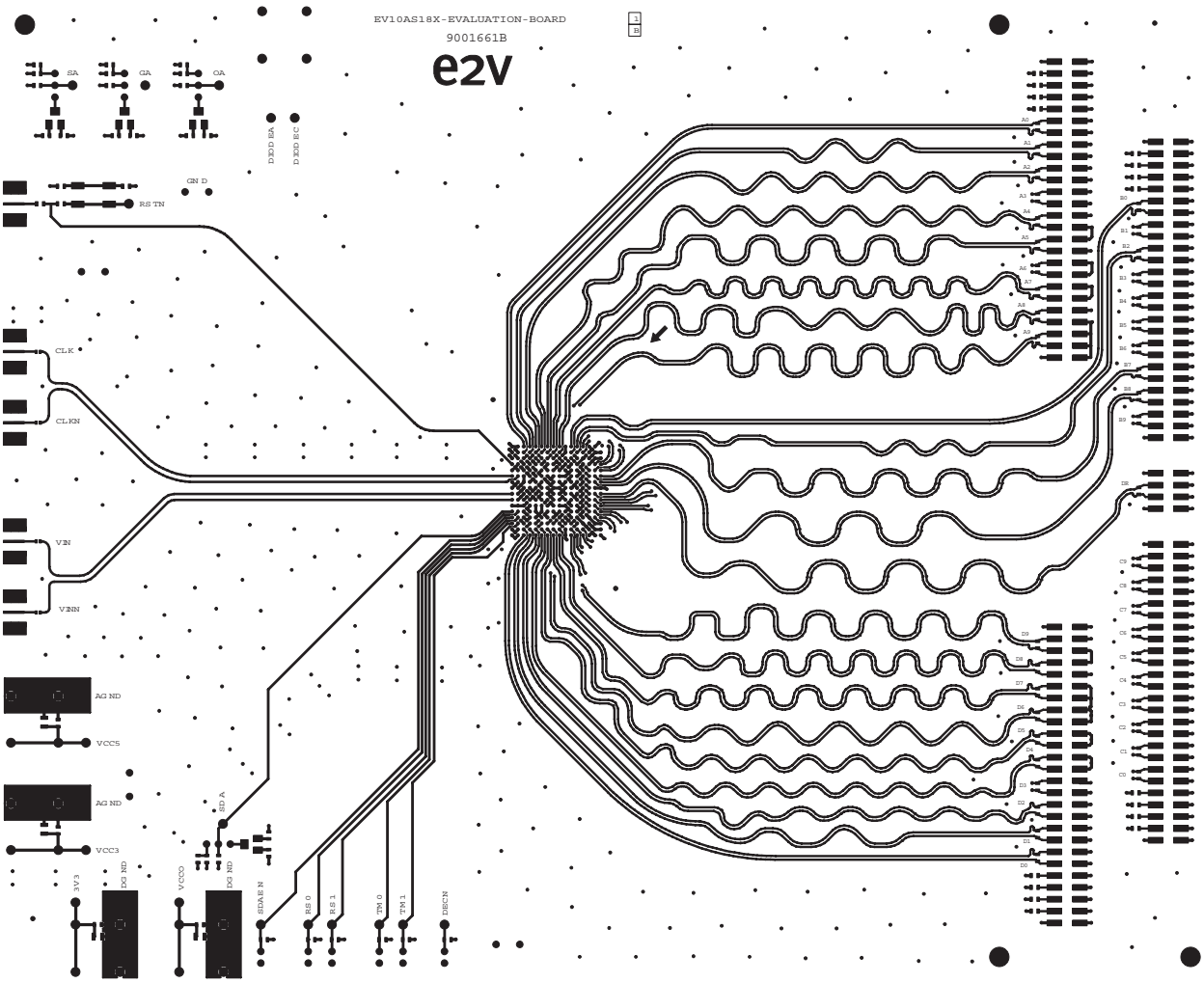
PORT B

Figure 6-6. Electrical Schematics (Output Connectors Ports C and D)



6.2 EV10AS180x-EB Board Layers

Figure 6-7. Top Layer



EV10AS18X-EVALUATION BOARD LAYER 1 COMPONENT SIDE

Figure 6-8. Bottom Layer

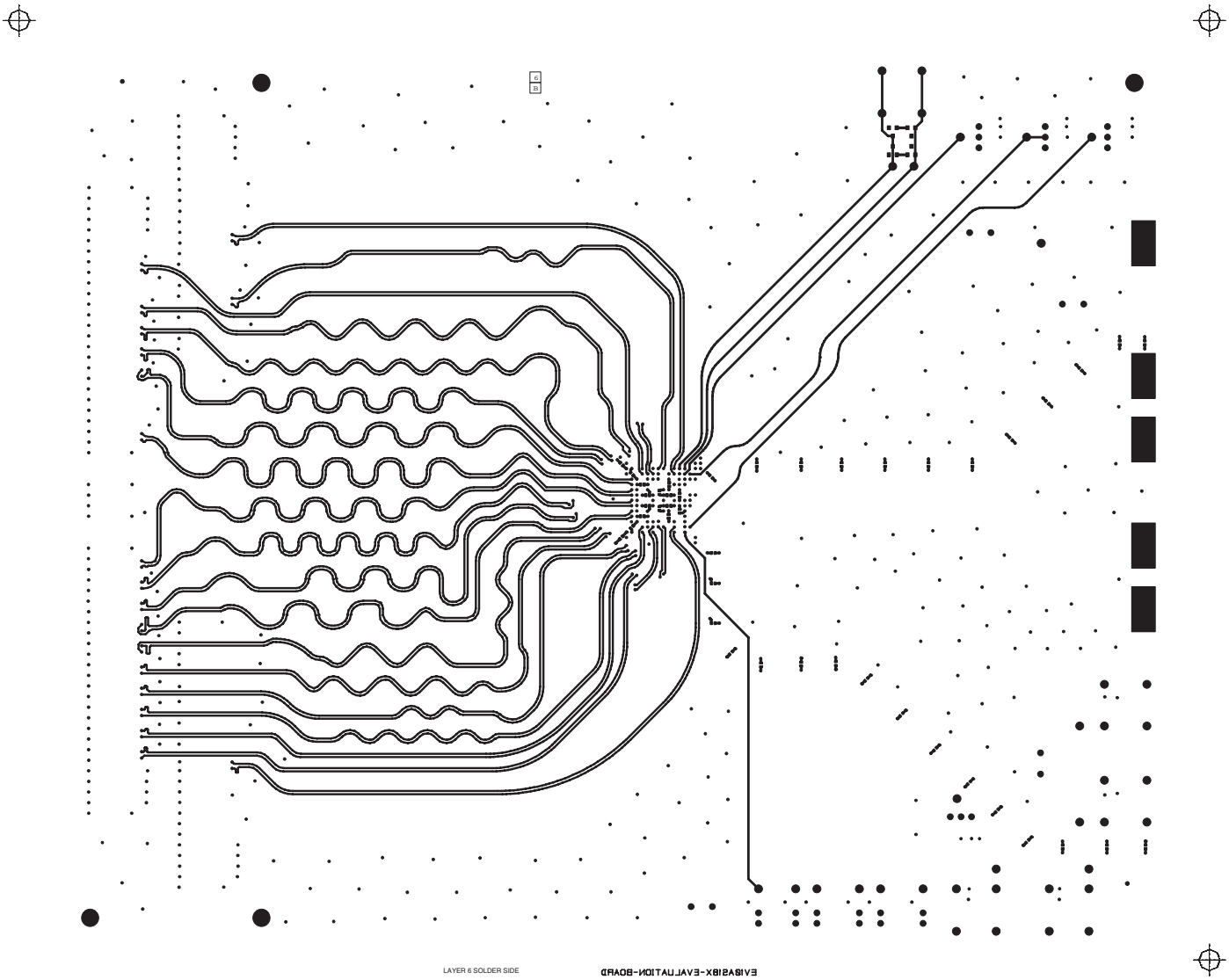


Figure 6-9. Equipped Board (Top)

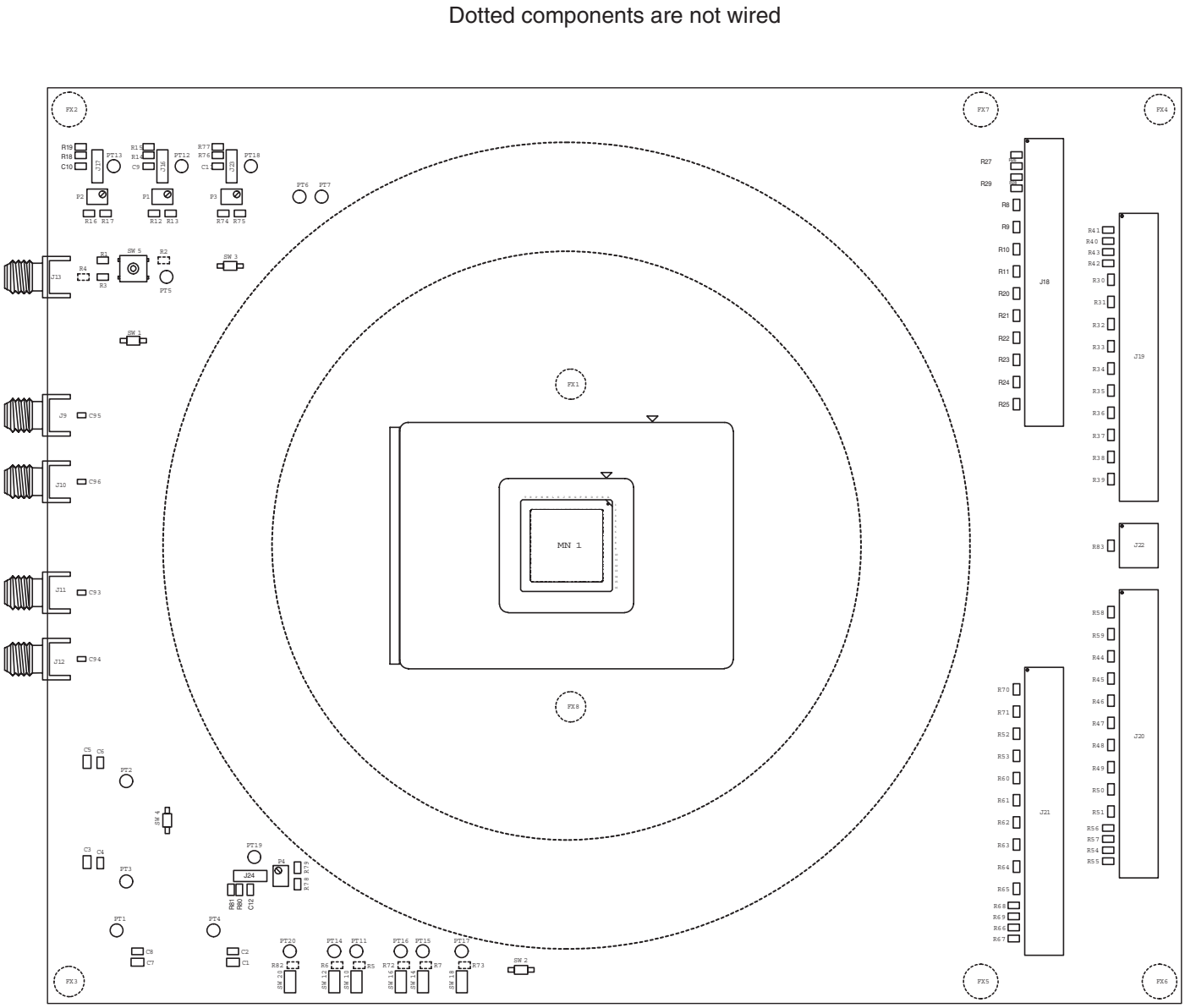
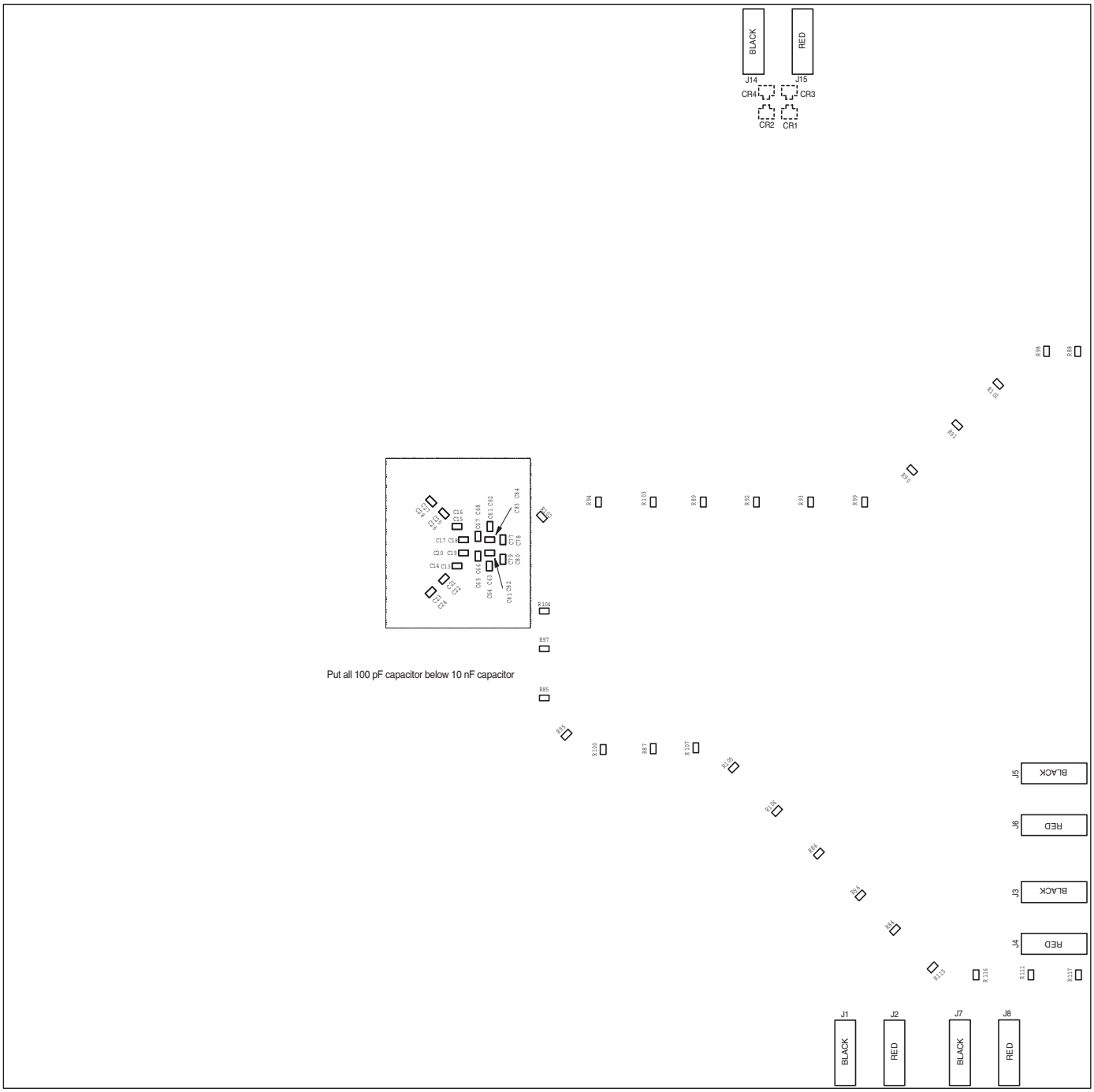


Figure 6-10. Equipped Board (Bottom)

Dotted components are not wired



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